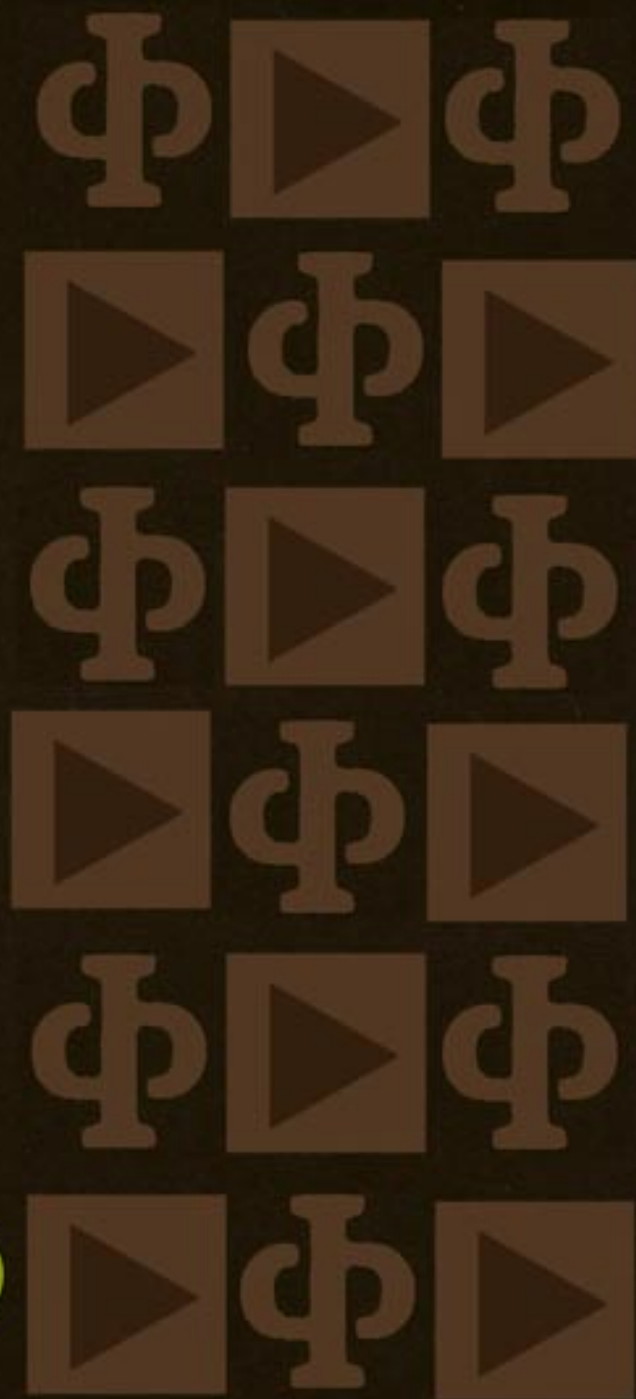


*Applications  
Manual for  
Computing  
Amplifiers  
  
for Modelling  
Measuring  
Manipulating  
& Much Else*

containing, in addition to frequent digressions into design philosophy, and numerous self-serving advisories on equipment selection, a library of practical feedback circuits

all employing modern Operational Amplifiers—mostly solid state—  
together with an occasional nostalgic, respectful, and useful reference to the not-yet-to-be-dismissed vacuum-tube art



PHILBRICK RESEARCHES, INC.



# WHO

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owner  
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George A. Philbrick Researches, Inc., founded in 1946, specialized originally as a manufacturer of systems and functional building blocks for analog computing. In 1952, the differential-input *operational amplifier*, a key analog component, was for the first time liberated from its functional setting and offered for sale individually. Following publication (1956) of the gray, 28-page *Applications Manual for Philbrick Octal Plug-In Computing Amplifiers*, created by MIT Professor Henry M. Paynter, amplifier sales mushroomed, rapidly outgrowing computer products.

By 1965, vacuum-tube devices like the K2-W were supplanted by potted modules employing discrete transistors; and the industry was introducing the first really performance-competitive ICs. But op amps lacked the support of suitable texts to educate, inform, and stimulate design engineers. In response, Philbrick devised this Applications Manual, using Ted Gams's unique modular approach to apportioning text and graphics to individual topics. Contributors included Dr. Peter Hansen, Bruce Seddon, Robert Malter, and Bob Pease; and the whole was edited by the undersigned. It was eagerly adopted and is fondly remembered by designers of an earlier generation.

Following the book's publication in 1966, Philbrick was acquired by Teledyne, Inc., and merged with a recently acquired competitor, Nexus Research Laboratory, Inc. In the early 1990s, it was merged with other Teledyne businesses and lost its identity. What remained of it became the property successively of TelCom Semiconductor and Microsemi Corporation.

Two generations of design engineers have appeared since the book's publication; the first generation to receive it is on the way to retirement or beyond. Good op amp books are now available. Yet many of the ideas expressed here remain fresh to this day. In fact, today's analog silicon may make feasible ideas that could once only be suggested but imperfectly embodied. The book has much that will be "news" to the newer generation. Approaching the millennium, Analog Devices, recognizing the book's possibilities, has acquired the rights to re-publish it. We have left it virtually unchanged, except for a few evident opportunities to make it more relevant to the current generation. We're delighted to have closed the loop—an eminently analog function!

*Dan Sheingold, Dec, 1997*



# WHAT

## APPLICATIONS MANUAL- COMPUTING AMPLIFIERS

This publication is the newest in what may reasonably be called a *publishing continuum*—a progression that began in 1951 with the appearance of our charming but (by today's standards) old-fashioned 36-page *Catalog and Manual*, revisions and mutations of which have appeared, along with *The Lightning Empiricist*, periodically throughout the intervening years. Your response to each of these *opera* has been warmly enthusiastic. Like Don Marquis's Mehitabel, we are always surprised and somewhat bewildered by the *magnitude* of the yield—for example, the "*Applications Manual for PHILBRICK Octal Plug-in Computing Amplifiers*", which this manual supersedes, first appeared in 1956, and to date we have printed and distributed about a quarter of a million copies, through ten editions. We must confess to a fond hope for a similar endorsement of this latest effort.

This manual was prepared by the Engineering Staff of Philbrick Researches.

# CONTENTS

**THIS MANUAL BEGINS**, quite properly, by justifying its existence (WHY . . . pp 3-4) and continues with a brief essay intended to ensure its efficient use (HOW . . . pp 5-6), following which the reader will find himself and his ambitions located in The Scheme of Things (WHEN & WHERE . . . pp 7-8)—thus, the entire task of Orientation requires only ..... **pages 3-8**

**PART I DEALS WITH FUNDAMENTAL CONSIDERATIONS**, and is designed to acquaint the reader with both the Capabilities of Ideal Operational Amplifiers and the Foibles of Practical Ones; and, by so equipping him, to anticipate and obviate the foibles, placing at his command the full power of the Analog Method . . . all of which occupies ..... **pages 9-38**

**PART II DESCRIBES COMPUTING CIRCUITS**, which have been divided, for sensible reasons, into circuits displaying:

*LINEARITY* ..... **pages 40-49**

*CONTINUOUS-FUNCTION NONLINEARITY* ..... **pages 50-55**

*DISCONTINUOUS-FUNCTION NONLINEARITY* ..... **pages 56-62**

**PART III IS DEVOTED TO INSTRUMENTATION AND FUNCTIONAL IMPLEMENTATION BY ELECTRONIC MEANS**, and is divided into five categories of opportunity:

*Energy Sources* ..... **pages 64-68**

*Signal Sources* ..... **pages 68-74**

*Filters* ..... **pages 74-78**

*Signal Conditioners* ..... **pages 79-84**

*Meters and Converters* ..... **pages 84-102**

**THIS MANUAL ENDS** (for now) with a set of Appendices intended for reference, guidance, and refreshment—before, during, and long after serious perusal of its many lessons. Included are:

*a Dictionary of NOMENCLATURE & SYMBOLOGY* ..... **pages 106-109**

*a BIBLIOGRAPHY of Worthy Publications* ..... **pages 110-111**

*AMPLIFIER OUTLINE DIMENSIONS* ..... **page 112**

*PHILBRICK PRODUCTS and SERVICES* ..... **page 113**

*and a COMPLETE SUBJECT INDEX* ..... **pages 114-115**



# WHY

The reason for this manual may be found in the nature of the Analog Art. As we shall soon relate, in the pages that follow, the successful application of that art often involves some degree of originality, is often improved by full-fledged creativity, and frequently demands genuine innovation.

Now we are not so naive as to believe that originality, creativity, or inventiveness may be taught, or even developed, *en masse*. In fact, we rather prefer this intractability of the human personality. Nevertheless, even routine applications of basic principles, clearly understood, can lead to successful, reliable, and practical results.

Not everyone, however industriously he reads this manual, will become a genuine Analog Artificer; but those who do so progress (and those who have already) will find that there is a close analogy between the study of a new language and the study of Analog Methods, to wit:

- A clear and complete understanding of the fundamental *rules* of the game (“grammar”) is essential to good performance.
- A thorough understanding of the laws of *combination and interrelationship* (“syntax”) must be acquired before any significant advanced work can be contemplated.
- The variety and scope of one’s output is directly proportional to the number of hard facts one has stored up about *available hardware* (“vocabulary”).
- The only way to avoid triteness and idiomatic clumsiness is to be exposed to a large number of successful, practical *solutions* (to be “well-read”).

To dwell on our analogy for one more paragraph, we should like to point out that, while a *superficial* knowledge of any language may be acquired by deliberately plunging oneself into the daily life of its country of origin, few are able unaided to overcome the intellectual barrier implicit in this pragmatic approach sufficiently to write or speak *professionally*. Our aim in preparing this manual, therefore, has been . . .

# WHY

(cont'd)

... to provide, not a Primer, nor even a "Dictionary of Useful Phrases", but rather *a course in how to think professionally—and creatively—in the language of Analogs.*

Those blessed with good habits of study and quick comprehension will, we trust, gallop through Section I at a fast clip. On the other hand, those for whom the pleasures of discovery have been spoiled (either by previous experience or by early exposure to other treatments) should not find our exposition without interest and merit—indeed, they are likely to uncover new and useful elements of technique.

Regardless of his status at page 9—sophisticate, savant, scholar, or seat-of-the-pants sluggard—every reader will find value in the library of designs contained in Sections II and III, as well as in the reference material in the appendices.

Furthermore, exposing our scarlet commercial stigmata, we have elected to specify for each circuit one or more Philbrick amplifiers, by type and even by their current model number. This move needs no special pleading . . . Philbrick amplifiers *are* really our first choice, always.



# HOW

WE SHALL NOT PRESUME to tell anyone how to read—or even how to study—a technical book. Everyone has his own method; indeed, he may have developed *several* habits, to suit different moods, climates, and objectives. Within reasonable bounds, this manual will accommodate and reward almost any kind of serious usage—from formal, systematic, cover-to-cover study to rambling and occasional scannings; from selective intense spot-reference, when a specific problem arises, to dilettante browsing, just for the fun of it. The uses of this manual are as varied, we believe, as the tastes and needs of its users.

EVEN THE CASUAL OBSERVER WILL BENEFIT, however, from a brief insight into the structure of this text, for it is unique in several ways, and must be used intelligently for maximum advantage. Few texts can and do bridge the gap between a continuous tutorial exposition and a reference work. This one does, we warrant, and we invite the reader's consideration of how to enjoy its versatility, before plunging into it.

An important part of the organization plan is the *grouping* of the material, which is shown below and outlined in some detail on page 2.

WHO, WHAT, WHY, HOW, WHEN, & WHERE: pp. 1-8

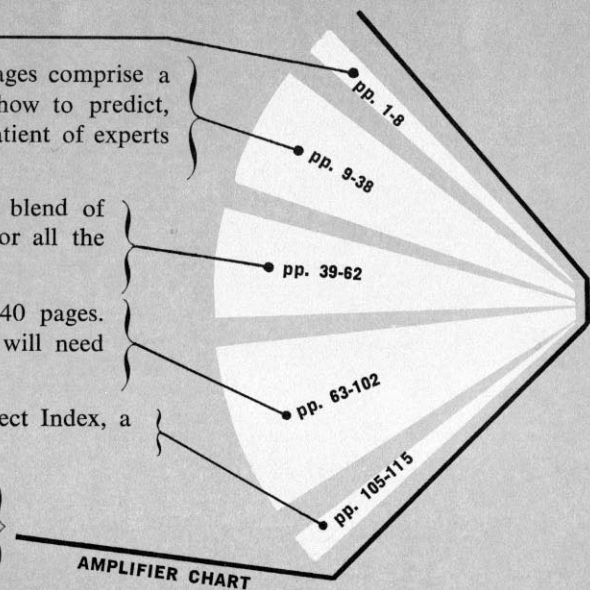
FUNDAMENTAL CONSIDERATIONS—not at all the same as “*elementary* considerations”, these 30 pages comprise a clear and rigorous exposition of how to make amplifiers perform in Operational Amplifier circuits, and how to predict, evaluate, and adjust their performance in practical circuits, under realistic conditions. All but the most impatient of experts should read this section through at least once, before setting pencil to paper with a specific application.

COMPUTING CIRCUITS cover the next 24 pages. The early sections of this part of the manual are a blend of tutorial exposition and applications advice; they should be considered as a source of background theory for all the rest of the text.

INSTRUMENTATION and other forms of functional IMPLEMENTATION are covered in the next 40 pages. Despite elaborate cross-referencing (explained later), the reader should stay alert to the possibility that he will need to lean on earlier material to develop a complete understanding of circuit theory and practice.

THREE IMPORTANT APPENDICES are contained in the last twelve pages—including a complete Subject Index, a Bibliography, and a Dictionary of Nomenclature and Symbology.

FINALLY, so that the word “Amplifier” will have more than symbolic substance and be realizable in specific, measurable terms, a chart of typical Philbrick Amplifiers is included, in fold-out format, so that relevant amplifier designations may be before your eyes as you study circuit diagrams and descriptions.



NOW AS TO THE *INTERNAL* ORGANIZATION.....

(cont'd)

# HOW

(cont'd)

A MANUAL or handbook differs from a textbook in that it must be designed to permit *random access* to the information it contains, yet the order and logic of its exposition must not be entirely sacrificed for the sake of either brevity or speed of search. The key to success, in both the writing and the reading of such a work, is a healthy respect for the *organization* of its contents; and the two most powerful tools available for organizing the written word are graphical design (layout) and inter-referencing. Learn how a manual is organized, and you are in a position to get much more out of it, faster and more accurately, than by picking it up and using it.

MOST OF THE INFORMATION in these pages is presented in modular form, the basic modulus being one third of a page, like the sample shown here. Sometimes a double or even a triple module is required, but most Sections conform in design to this sample.

**Text frequently contains cross-references by Section number. Be sure to scan the text for these, since their particular significance is not indicated in the listings below the Section number, on the right-hand edge of the page.**

**Section Number and Title.** (Number is repeated on right-hand edge of page.)

**III. 12 TWO-PHASE OSCILLATORS**

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---

$$e + T^2 \frac{d^2 e}{dt^2} = 0 \quad (3-7)$$

---



---

$$f_n = \frac{1}{2\pi T} = \frac{1}{2\pi RC} \quad (3-8)$$

---



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**Equations are numbered sequentially within each Part—e.g., equation (3-7) is equation #7 in section III. This equation is always so numbered, regardless of where it may appear later.**

**The schematic and block diagrams are referred to by section and (if necessary) by a sub-letter. The lower diagram shown here is called figure 3.12 (b).**

**Footnotes—often vital to successful implementations of circuit. Always check these footnotes before attempting to apply the circuit suggested!**

**3.12 (a)**

**3.12 (b)**

$$f_n = \frac{1}{2\pi RC}$$

**Section Number in bold print. The Roman numeral is the Part number (I,II,III) and the arabic numeral following the decimal point is the Section number within that Part.**

**Reference Number(s) in light print. These are provided to ensure that non-repeated material is made available to you, even if you have not read earlier or later parts of the text.**

A FEW MINUTES DEVOTED to memorizing the disposition of data within the Section will be found very worthwhile. Likewise, a few minutes spent in familiarizing one's self with the Appendices (pp. 105-115) would be well invested. After that, you are ready to move mountains!

6



# WHEN & WHERE

What are the uses of the Analog Art? When and where should the Analog Artificer be called upon to practice his magic? We know of no better way to begin to describe the rightful provinces over which this specialist reigns than to reproduce here, from an earlier work, two paragraphs that have frustrated all attempts at improvement, over the decade since they were written:

## ANALYSIS and ANALOGY

If Mathematics can be called the "Queen of the Sciences", then truly Analogy is her consort. When logic is enlivened, existence theorems become self-evident.

By introducing *amplifiers* into physical structures, to supply activation energies while enforcing signal flow causality, unlimited realms of abstraction may be physically realized. This does not mean, however, that Fictions may be made Truths; indeed learning to flatter rather than antagonize Nature is part and parcel of the Analog Art.

Specifically, using active circuits, one may construct an *Electronic Analog Computer*, a device using voltages to represent all variables. Such computers are used as research and development tools in the design and operation of industrial process controls, chemical reactions, electrical networks, and complex military systems, among others. They have especial value for dynamic systems, where vibration, stability, and response time are major design factors.

If relations and parameters are known, computation is a straightforward problem of solving algebraic and differential equations. However, analog computers also permit studies of systems where relations describing performance are not clearly known in advance. In this case, portions of the system may be *simulated* by active or passive networks constructed experimentally to give a behavior approximating known or desired response. Here operational amplifiers are used, for example, as isolating and amplifying elements between stages, scaling elements, lag or delay components, oscillators, regulators, as well as for basic mathematical operations.

However they arise, all computer representations of real or abstract systems are physical *Models*, but of extraordinary flexibility.

## CONTRIVANCE and CONTROL

Even a few moments with these tools in hand leads one to attempt to better the pallid past and attune with a fruitful future. The seeming vices of material processes can be turned to virtues through union of energy and entropy control. Lags can be made leads to predict the probable future from the known past. Instrument bridges may be monitored and balanced with continuous accuracy. Response data of processes may be digested immediately to enhance research and reward industry.

In electronic portions of closed-loop control systems and servomechanisms, operational amplifiers can be used as *brains* to command the *muscles*. The "error" between the ideal or desired condition and the existing condition is constantly measured by an input amplifier, and then (sometimes using the same amplifier) is amplified, transformed, scaled, and applied through power actuators to the process under surveillance as a corrective force to reduce the error. Stabilizing and compensating networks are conveniently implemented through subsidiary feedback operations.

In addition to the direct control applications indicated above, operational circuitry has been profitably used to simulate processes for testing and shakedown of prototype control systems and conversely for simulating projected controllers by actually operating existing plants, processes, or machines. Such uses have already enjoyed remarkable success in engine design and prime mover development; comparable promise is indicated in other fields.

The above realms briefly indicate possibilities of *instrumental* applications, wherein input signal information is transformed continuously into directly useful open or closed-loop output actions.

The *computation, simulation, measurement, and control* of physical parameters, then, are the domains in which the Analog Artificer may most effectively function. In this manual, we are chiefly concerned, as we have explained earlier, with *how* he achieves his results. For a guide to more elaborate *descriptions* of such results, see the **Bibliography**, pp. 110-111. (cont'd)

# WHEN & WHERE

(cont'd)

Analogies are made possible by nature's wonderful system of structural parallelism in which a physical element in one medium may be represented by a corresponding physical element in another (e.g. mechanical *mass* may be represented by electric *capacitance*).

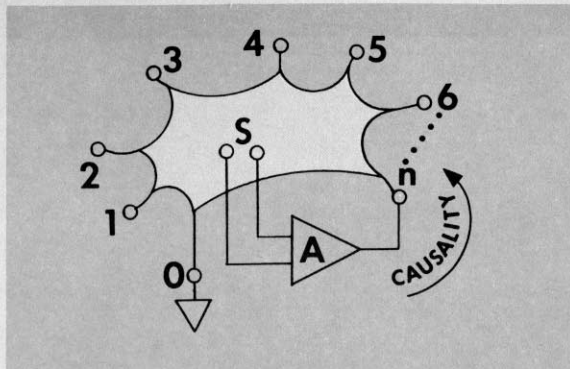
Analogs are most helpful when an inherently inflexible system, or a system of great cost, or one of unknown performance, is to be investigated. A problem may be rewritten so that, in effect, the story remains the same but the names of the characters are changed; or, more specifically, an Analog may be set up in a more convenient system. The time scale may also be changed to suit one's convenience.

There are two basic forms of Analogs: *passive*, in which flexibility is limited by the physical realizability of passive Networks; and *active*, in which the Amplifier extends the limits of realizability, by a bit more each year, as circuit techniques improve and the state of the component art advances. (The *electronic* Analog is clearly superior to that created in any other physical medium. Electronic Analogs offer far greater parameter ranges, greater flexibility of configuration, higher speeds and accuracies, all at lower cost.) "Mixed" Analogs exist, in which the amplifier merely extends the range of a passive Analog; e.g., by impedance transformation.

## ACTIVE ANALOGS

The active Analog can be made by activating a passive Network and may be represented generally by the drawing to the right.

The shaded area represents any physically-realizable, isolatable Network (often passive) in any medium, having terminals 0, 1, 2, 3, . . . , and a node-pair or *Null* (i.e., an energy equilibrium) at S.



The triangle A is an amplifier (hydraulic, pneumatic, mechanical, or other) having high gain and a net reversal of sign (polarity or "sense"). The null in the Network is maintained by A because any energy difference at S (the *input* to A) is always  $(1/\text{gain of A})$  of the *output* of A (the apex of triangle). Thus, the resultant of the efforts applied to the Network will be nullified at S, and the force at point *n* (the output of A) is determined only by the Network and the efforts applied to the Network.

"The Method", then, consists of applying the principle of the Active Analog in one or more of several different ways:

- **By Modelling**—that is, given a particular device or devices, in a particular physical system, and one or more questions about its behavior under a given set or sets of conditions (external forces—0, 1, 2, . . . *n*), one constructs a convenient electronic model, applies analogous external forces (signals, bias voltages or currents) and then makes a sufficient number of observations, of both magnitude and magnitude-vs-time, to answer the questions posed in the problem statement. (It is, of course, necessary, in constructing the model and making the observations, to use "hardware" that will ensure a degree of accuracy consistent with the problem statement.) One particular kind of modelling—the best-known kind, perhaps—is *mathematical* modelling, known as computing.

- **By Synthesis**—that is, given a general description of the *nature* of the device to be synthesized, and a set of answers (performance specifications), one constructs an Active (or passive Analog of the general type described in the problem statement, and adjusts its parameters until the stated performance is observed—once again, with an intelligent and watchful eye on the accuracy levels maintained in both hardware and measurement. (It should be noted that all too often the "general description" of the device given in the problem statement is *too* general, and a certain amount of inspired creativity is required of the Analog Artificer. We trust that this fact cheers and reassures you as to the importance and contribution of the individual—as it does us.)

- **By Pure Implementation**—that is, given little or no restriction on the nature of the device, but only a performance requirement (generally less than complete), one constructs what one hopes is an elegantly simple Analog that will respond to external forces in the prescribed manner. Both instrumentation and control, in all their glorious scope and variety, fall into this class of creativity . . . and the book will never be closed, we trust, on mankind's record of accomplishment in playing this exciting game. (Although it occasionally causes painfully expensive redesign, every significant improvement in componentry and circuitry creates a new "set of rules" for this game, adding immeasurably to the spice of our lives—and, we trust, yours.)

The reader should not, if relatively new to this fascinating Approach to Life, feel either alarm or inadequacy at this stage. Rather, he should blame the limitations of written communication, particularly as practiced (however fervently) by us, for any sense of incomplete understanding. Read on—and then return, when the mechanics of this Analog business are more familiar, and read this statement again. We predict that, as it does so often in Nature, courage will follow competence.



# PART ONE

## FUNDAMENTAL CONSIDERATIONS

Modules	Pages
I.1-I.6 Primary Concepts—Ideal Performance.....	10-12
I.7-I.18 Departures from Ideal Performance— Ills & Cures.....	13-19
I.19-I.27 Circuits for Approaching the Ideal.....	20-24
I.28-I.31 Interface Philosophy and Technique.....	25-26
I.32-I.39 The Tools of the Trade.....	27-30
I.40-I.46 Setting Up Working Circuits.....	31-34
I.47-I.51 Measuring Amplifier & Circuit Performance.....	35-37
I.52 Notes.....	38

**I.1 OPERATIONAL AMPLIFIERS.** An amplifier that activates a passive Network to form an active Analog is called an Operational Amplifier. It is this amplifier that enforces the Null in the Network, and allows the Network to impart to the performance of the combined circuit its own (passive) parameters.

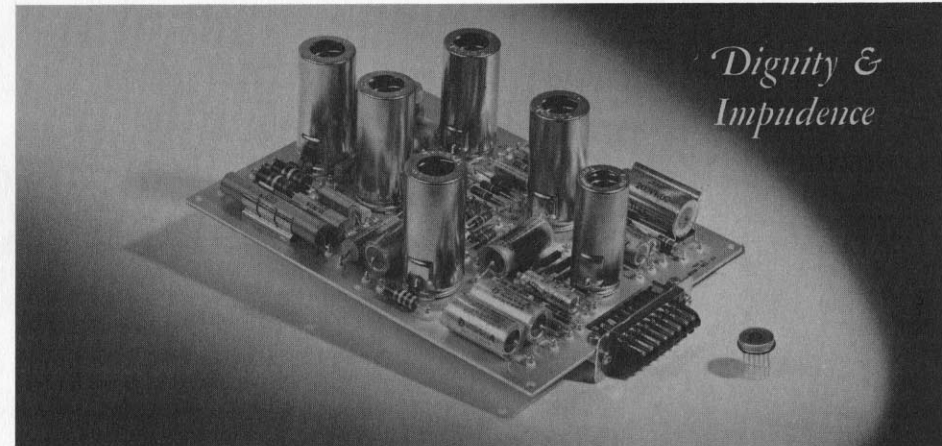
Practical Operational Amplifiers are characterized by extremely high “DC” (static) and low-frequency gain, so that the input (or “error”) signal required for full output is generally negligible, both in current and in voltage. General-purpose Operational Amplifiers are also characterized by low closed-loop output impedance, and by a fairly uniform roll-off in gain with frequency over many decades. As we shall see, this “linear” roll-off characteristic gives the operational amplifier its *universality*—the ability to accept feedback from a wide variety of feedback networks with excellent dynamic stability.

## EDITOR'S NOTE

A Dictionary of Nomenclature and Symbology will be found on pp. 106-9. A glance at it now, and occasional references to it in times of stress, might speed the reader's progress through these pages.

**I.2 ELECTRONIC AMPLIFIERS.** Both vacuum-tube and solid-state Operational Amplifiers are in wide use, although the number of solid-state units has already exceeded the number of vacuum-tube units still in service. Without in any way detracting from the glorious record established by Philbrick vacuum-tube amplifiers, it is manifest that modern solid-state circuits have by now almost eclipsed that radiance. The day of the vacuum-tube Operational Amplifier may not be over, but it is Twilight . . .

Solid-state or Vacuum-tube, the Rules of the Game are immutable. Designing and manufacturing dependable yet economical Operational Amplifiers demands the greatest care—from circuit selection and component quality assurance to flawless workmanship under controlled conditions. If the “Solid-State Revolution” has changed any of the Rules, the effect has been to make Philbrick's depth of experience, design integrity, and vigilance even more important.



I.2

1.37

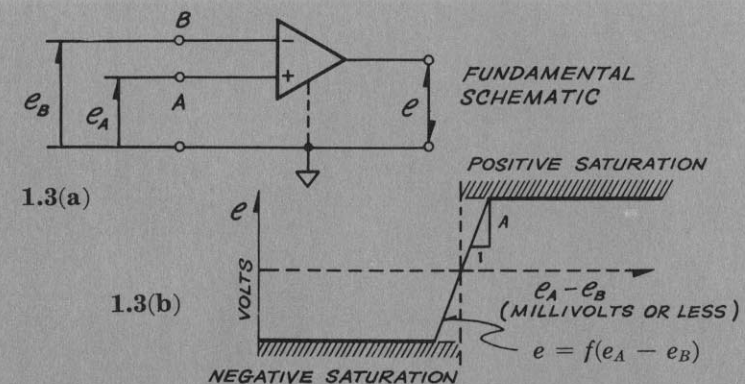
1.38

1.39

**I.3 FUNCTIONAL DESCRIPTION OF AN AMPLIFIER.** The schematic symbol of an Operational Amplifier, shown here, is a triangle that indicates the causal direction of signal flow. A ground reference is implied by the dashed lines. Almost all Philbrick Operational Amplifiers are provided with balanced inputs, “A” and “B”, to which are applied the input signals,  $e_A$  and  $e_B$ .

The output,  $e$ , of an operational amplifier is related to its inputs by\*  $e = f(e_A - e_B)$  as indicated on the graph to the right. A useful output signal may be obtained by applying a minute signal ( $e_A - e_B$ ) between the input terminals; in fact, the amplifier output circuit can be saturated by a surprisingly small input. The slope of the non-saturated portion of the characteristics determines the DC gain,  $A$ .

\*ignoring certain important error-factors, for which see I.7, I.18, and I.52.



I.3

1.4

1.7

to

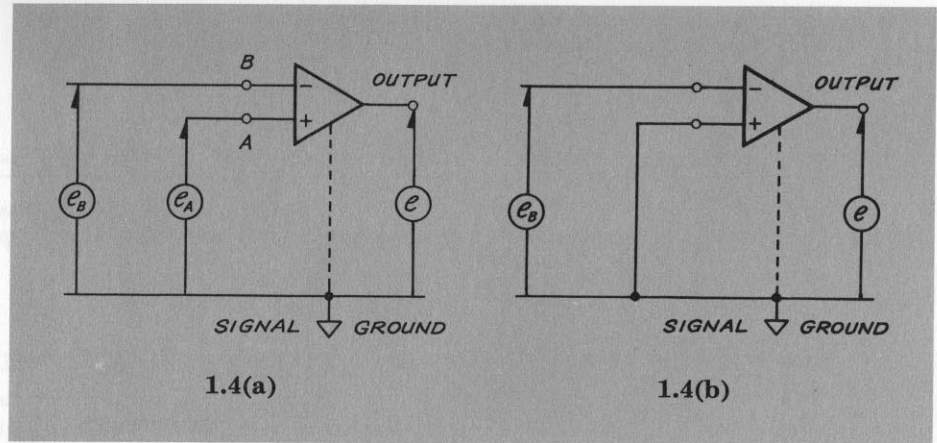
1.18



**1.4 AMPLIFIER INPUT CONFIGURATIONS.** Almost all Philbrick Operational Amplifiers provide balanced, differential inputs, as in (a), except for certain chopper-stabilized types, which are single-ended, as in (b), requiring grounding of the (+) terminal. Ideally, the output of (a) is:

$$e = f(e_A - e_B) \quad (1-1)$$

so that the output is independent of the *magnitudes* of either  $e_A$  or  $e_B$ , but depends only upon their *difference*. For example, if  $e_A = 10$  volts and  $e_B = 10.002$  volts, then the *effective* input is  $-2$  millivolts, just as if  $e_B = 0.002$  volts, and  $e_A$  were zero. Calling 10 volts the “common-mode voltage,” or CMV, an ideal differential amplifier would reject the common 10 volts, responding *only* to the 2 mv difference. In practice,  $e_A$  and  $e_B$  are hardly ever given *exactly* the same weight (see I.16 for discussion of common-mode error).



I.4  
I.7  
I.8  
I.16  
I.18

**1.5 TWO EXEMPLARY CIRCUITS.** The time has come to introduce a *circuit*. We are not quite ready for a completely *practical* circuit, but we may now consider an *idealized* application—a peg, if you will, on which to hang impending discussions of practical circuits.

Circuit (a) is the popular and useful “unity-gain inverter”, in which the output is (ideally) equal to and opposite in sign from the input. We are here only concerned with *how it functions*, ideally.

The ideal amplifier has infinite gain and infinite input impedance, draws zero input current ( $i_s$ ), has zero output impedance, zero propagation delay, and a completely passive input . . . that is, it does not *generate* signals. Pickup is zero,  $R = R_1 = 10k\Omega$  exactly, the power supply furnishes perfectly-constant noise-free DC, adverse environmental influences are absent, the Lark’s on the wing, etc.

Since  $i_s$  is zero,  $i_1 = i_2$ , by Kirchoff’s Law, taken at the summing point. With infinite gain, no input signal, however small, would be tolerated by the feedback, so that  $e_n = 0$ , terminal A is at zero, and  $e_s$  is also zero. From the above, we may develop a “Response” equation:

$$i_1 = \frac{e_1}{R_1} = i_2 = \frac{-e}{R}$$

or

$$e = -e_1 \left( \frac{R}{R_1} \right) \quad (1-2)$$

In Figure 1.5(a), we have assumed quite arbitrarily an input signal that varies with time (in an asymmetrical manner, for clarity) and have indicated, in three small graphs, the variations with time of  $e_1$ ,  $e_s$ , and  $e$ . How sweetly simple is the ideal!

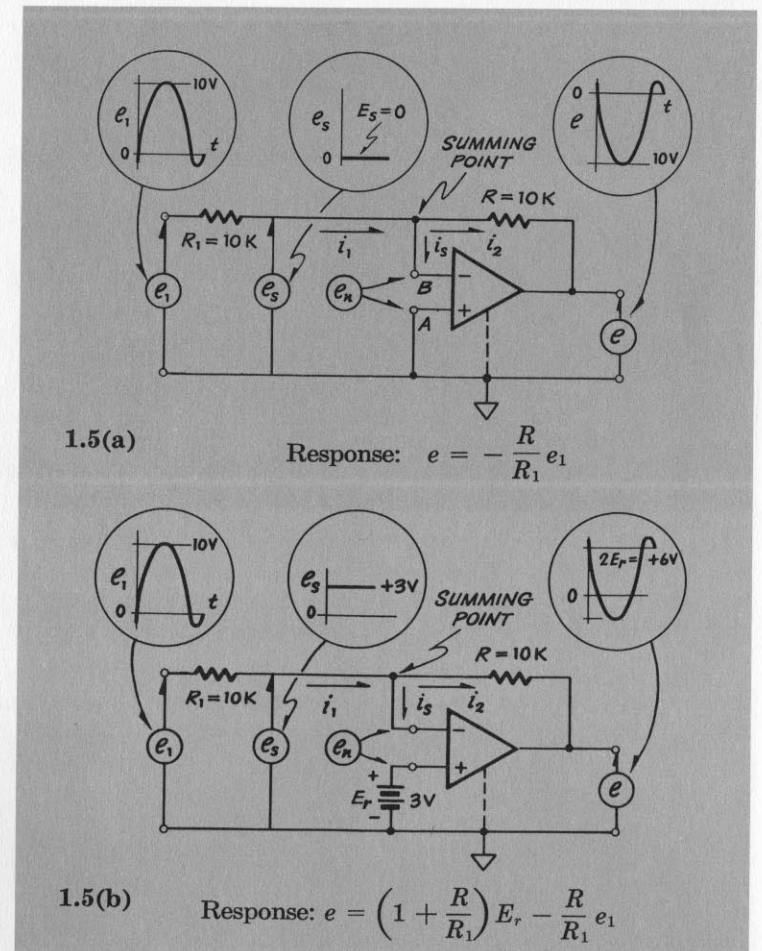
In circuit (b), we introduce a minor but important variation, in which a signal,  $E_r$ , is introduced into the positive terminal of the amplifier. Circuit (a) uses the amplifier in a single-ended manner; circuit (b) uses its differential configuration fully. By the way, we choose a battery for  $E_r$  for simplicity only.  $E_r$  could vary just as arbitrarily as  $e_1$ , without altering our analysis. The Response equation for (b), based on the same idealistic assumptions as for (a), is:

$$i_1 = \frac{e_1 - E_r}{R_1} = i_2 = \frac{E_r - e}{R} \quad (1-3)$$

or, if  $R = R_1$ ,  $e = 2E_r - e_1$

We have assumed that  $e_n$ , often called the “null voltage”, is zero, and that the gain infinite. Beginning with I.7, we shall face the facts: that the gain *is* finite, and that  $e_n$  is *not* zero, but is possibly appreciable, having the value  $-e/A$ .

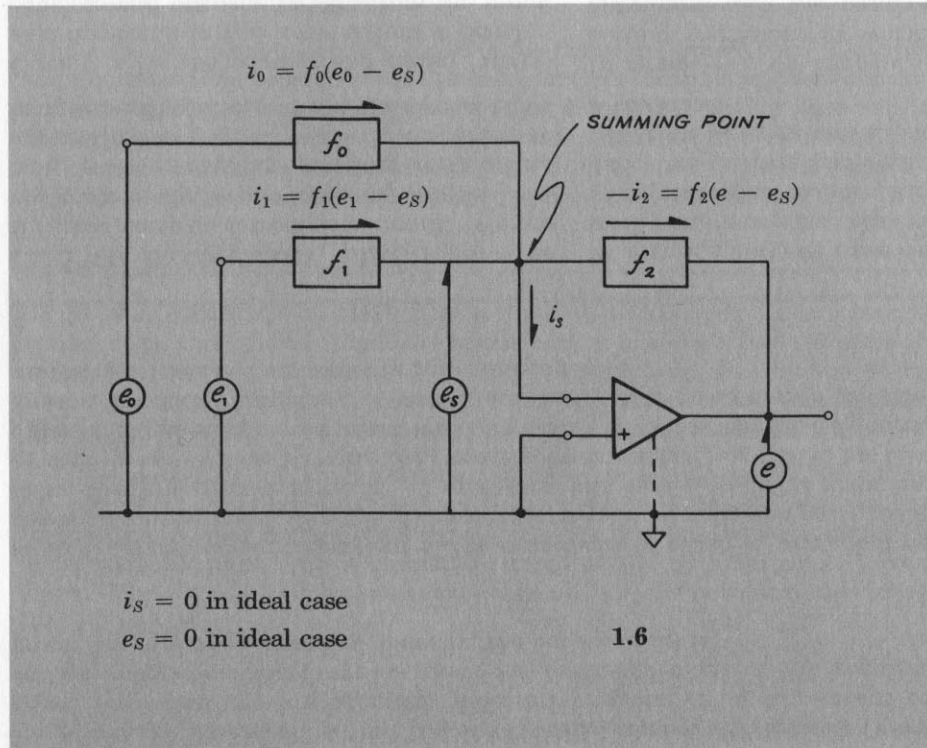
To sum up: in (a),  $e_1$  is perfectly reproduced, with inverted sign; in (b), we have linearly combined *two* signals,  $e_1$  and  $E_r$ , in accordance with equation (1-3). Both circuits generate currents ( $i_2$ ) precisely proportional to the difference of the input signals, if  $R_1$  is linear.



I.5  
I.6  
I.7  
to  
I.18  
I.40  
to  
I.44  
II.1

**I.6 GENERAL OBSERVATIONS ON IDEAL CIRCUIT PERFORMANCE.** Since we shall, (like all philosophers) make frequent reference to the ideal when discussing the non-ideal, we have elected to use as the prototype of all ideal circuits a somewhat-generalized application circuit, not too far removed from the example just considered in 1.5(a). In this generalized circuit,  $e_0$  and  $e_1$  are applied to the summing point of an Operational Amplifier circuit through two-terminal\* networks having the bifilar (linear or nonlinear) transfer properties described by  $f_0$  and  $f_1$ . The output,  $e$ , is connected (fed) back through a Network having the transfer properties  $f_2$ , to the same point—a point at which, please note, a virtual *null* or zero potential with respect to ground is forced to exist by the feedback of the output voltage developed by the Operational Amplifier . . . thus effectively isolating the input networks from one another and from the output, despite their connection.

\*For pedagogical simplicity.



Since an ideal case deserves an ideal amplifier,  $i_s = 0$ ; therefore  $i_0 + i_1 = i_2$ , as before.

Now then—let us particularize as we did in I.5: assume that the gain of the amplifier is infinity for all frequencies of importance in the time-domain responses of  $f_0, f_1$ , and  $f_2 \dots$  to which frequency range we also restrict  $e_0$  and  $e_1$ , and assume further that the circuit is stable.

If we now assign a form to  $f_0, f_1$ , and  $f_2$  (not a *value*, but merely a *form*) by assuming that they are linear admittances given in operational form\* by:

$$f_0 = \frac{1}{Z_0(p)}, \quad f_1 = \frac{1}{Z_1(p)}, \quad \text{and} \quad f_2 = \frac{1}{Z_2(p)}$$

$$i_0 = \frac{e_0 - e_s}{Z_0(p)}, \quad i_1 = \frac{e_1 - e_s}{Z_1(p)}, \quad \text{and} \quad -i_2 = \frac{e - e_s}{Z_2(p)}$$

we can derive a fundamental relationship between  $e$  and  $e_1$ :

$$\frac{e_0 - e_s}{Z_0(p)} + \frac{e_1 - e_s}{Z_1(p)} = \frac{e_s - e}{Z_2(p)}$$

which reduces, when  $e_s$  approaches zero (because of the high gain) to:

$$\frac{e_0}{Z_0(p)} + \frac{e_1}{Z_1(p)} = \frac{-e}{Z_2(p)} \quad (1-4)$$

$$\text{or} \quad -e = \frac{Z_2(p)}{Z_1(p)} e_1 + \frac{Z_2(p)}{Z_0(p)} e_0$$

which relationship also depends upon two less obvious assumptions: that the amplifier is able to produce the necessary output current, including  $i_2$ , and that  $e$  is within its bounds.

Three additional fundamental relationships are already within our grasp:

$$i_0 = \frac{e_0}{Z_0(p)}, \quad i_1 = \frac{e_1}{Z_1(p)}, \quad \text{and} \quad i_2 = \frac{-e}{Z_2(p)} \quad (1-5)$$

demonstrating that each input current is constrained to depend *only* on the voltage applied to that input.

\*The operator  $p$  is defined as follows:

$$y = \frac{dx}{dt} \equiv px$$

$$x = \int y dt = \frac{y}{p}$$

For sine waves,  $x = X \sin \omega t$

$$px = \omega X \cos \omega t, \quad \text{and}$$

$$p^2 x = -\omega^2 X \sin \omega t$$

Hence,

$$p = \sqrt{-1} \omega \equiv j\omega$$

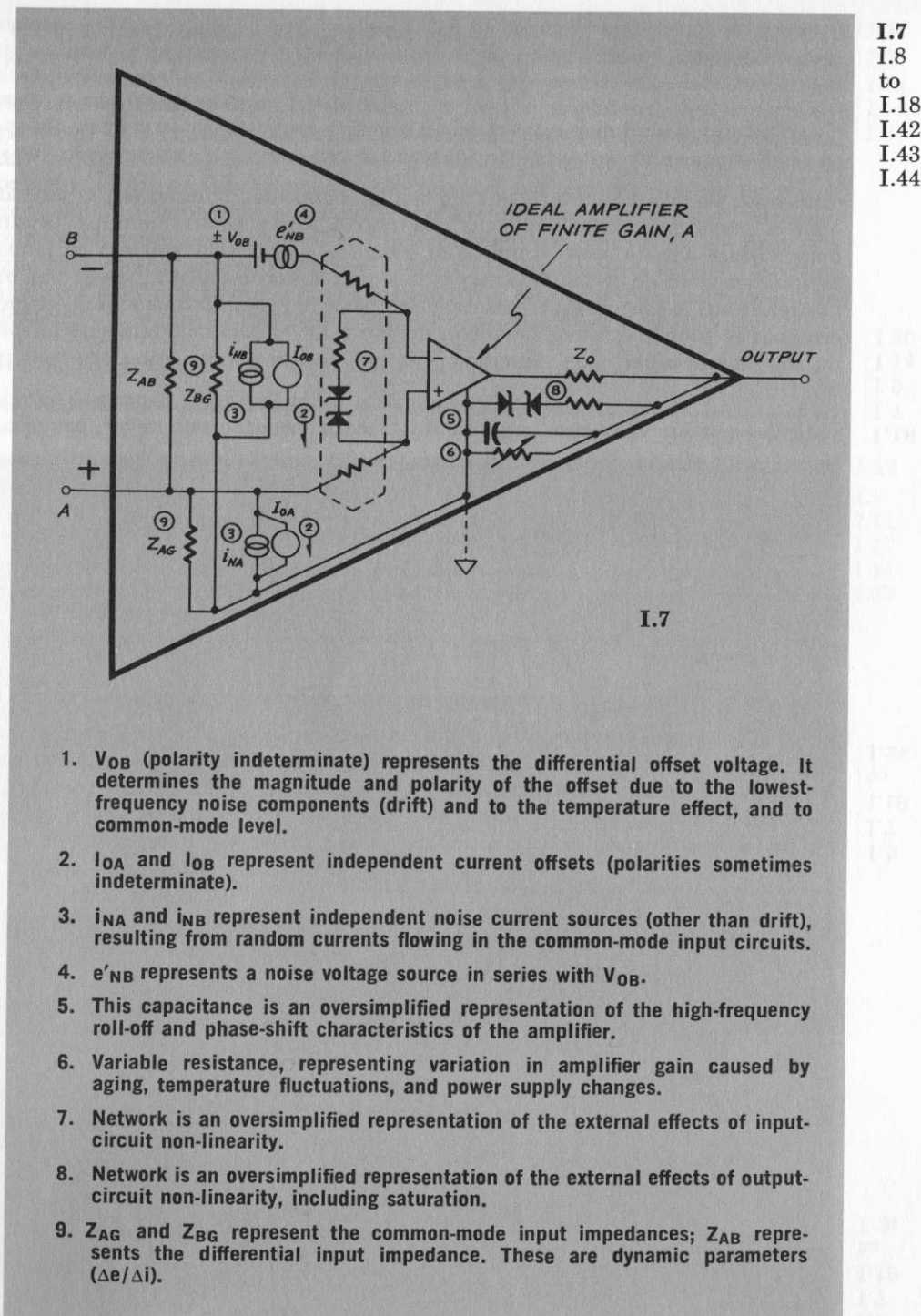


**I.7 DEPARTURES FROM THE IDEAL.** Does anyone ever grow so experienced that he recognizes and allows for *every* possible imperfection in Nature's real version of Man's idealization of Her? We doubt it; nevertheless, we make bold to list hereunder the imperfections in Operational Amplifiers that will be found to have primary significance in the practice of the Analog Art:

- **Voltage and Current Offsets** . . . Offsets are usually small, undesired signals generated by the amplifier and appearing at its input (see I.8). They can never be *perfectly* biased away, except at one moment in time, under one particular set of conditions. (Sections I.19–I.23 will assist you in striving toward perfection.)
- **Drift** . . . slow changes in offset with time/or temperature, soon (I.11 & I.12) to be confronted with courage and (consequent) competence.
- **Noise** . . . soon to be defined and dealt with (in I.9 and I.10). Drift, by the way, is one form of noise . . . the lowest-frequency component of the noise spectrum, which includes other pests, such as hum, flicker, hash, etc., etc.
- **Non-Ideal Amplitude and Phase Response vs. Frequency** . . . concerning which, see I.17 and the later section on Dynamic Stability (I.42). Limitations in the open-loop Gain and Phase performance of an amplifier are actually important imperfections in its *Gain Characteristic*. Less important imperfections include variations in gain with time, temperature, and power-supply voltage.
- **Non-Ideal Impedance Levels** . . . one aspect of this class of imperfections is less-than-infinite input impedance, or its complement, higher-than-zero output impedance; another aspect may be unbalance of impedances, causing asymmetrical behavior in differential amplifiers; finally, there is the question of *non-linear* impedances (I.18). For each of these ills, there is, within reason, a cure.
- **Input and Output Limitations and Non-Linearities** . . . whenever the mathematics (which deals with abstractions) calls for circuit performance beyond the specifications (which arise from realities) one or more non-linearities will be discovered. These are treated (with respect and practical advice) in many sections.
- **Common-Mode Error** . . . a subject broached in section I.4, and dealt with squarely in I.16.

Finally, we must mention a factor that contributes to error—to departure from ideal—in every application, yet may hardly be termed an “imperfection”: the fact that the gain of a practical Operational Amplifier is not infinite. Because it is not, we may never obtain elegantly-simple mathematical results *exactly*, but we may only *approach* them . . . in most cases to an accuracy limited *only* by that of the passive components in the circuit. (more on this in I.15)

The above concepts are graphically and schematically illustrated to the right. Before leaving this stimulating subject, the reader should note that *compounds* of the above phenomena are also possible; e.g. *Rate Limiting*—a form of *dynamic* non-linearity, in which amplitude-non-linearity at some point in the amplifier circuit conspires with its frequency-response characteristic to produce a limitation on the maximum rate of change (or *slewing rate*) of output signal. *Courage!*



**I.8 OFFSET AND BIASING.** In all DC amplifiers, a small, relatively-constant (but temperature-dependent) voltage, called “offset,” appears between the two input terminals. It may be thought of as a small voltage in series with one or the other of the input leads. In solid-state models, offset is usually well within a millivolt, over long periods and moderate temperature ranges. Most solid-state designs are available with a screwdriver-settable zero adjustment. If internal adjustment is not provided, or remote adjustment is desired, some form of adjustable zero-setting bias voltage may be employed; see I.19–I.23.

All amplifiers also demand some small and relatively-constant current at each input. In some designs, this *offset current* can be made as low as  $10^{-13}$  amperes; in other designs, it may be a fraction of a microampere. In many applications, offset currents may be neglected, and bias-current supplies (I.20–I.23) are unnecessary.

In other applications the amplitude and stability of offset currents or voltages are the most important criteria in the selection of an amplifier.

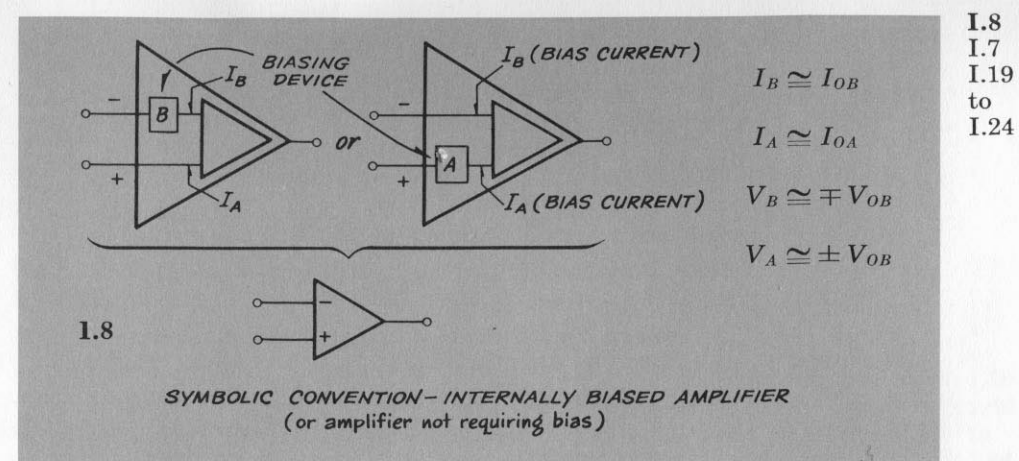
**I.9 CLASSIFYING NOISE.** The term “noise” as used here is all-inclusive, embracing all spurious or unwanted signals (offset and temperature drift excluded), random or otherwise, that are not correlated with any input signal.

It is customary to divide the noise spectrum into several frequency ranges, each of which tends to be dominated by certain noise components. For example, the “broadband” or “wideband” noise spectrum, which extends from 1 kHz to 100 kHz, tends to be dominated by resistor (Johnson, or thermal) and shot (semiconductor or vacuum-tube) noise. Both are readily predicted from simple theoretical considerations.

The noise spectrum from 10 Hz to 1 kHz tends to be dominated by pick-up (primarily capacitive) at power line (or chopper) and frequencies harmonically related thereto.

**I.10 NOISE PARAMETERS DEFINED.** In each of the noise bands described in I.9, amplifier-generated noise may be considered to be produced by the combination of a noise-voltage source in series with one of the inputs, and noise-current sources shunting each of the inputs to ground, the entire equivalent network synthesized in such a way that the root-mean-square noise voltage measured at the output is predictable regardless of the feedback network, provided, of course, that the noise contribution of the feedback network is either included in the reckoning or is negligible. These noise sources may usually be assumed to be completely independent of (or uncorrelated with) each other, without serious error.

The ratio of the root-mean-square noise voltage to the root-mean-square noise current of the equivalent sources is called the “characteristic noise resistance” ( $R_s$ ) of a noise source. A noise source may have a different value of noise resistance in each frequency band. If, at the input of an operational amplifier, the parallel combination of all input-circuit and feedback-network impedances



The range from .1 Hz to 10 Hz (“narrow band”) is usually dominated by (theoretically unpredictable) so-called “1/f” noise\*, or flicker associated with structural imperfections in components, particularly in (but not limited to) transistors. Below this range in frequency the dominant component is what we have called drift, and which we have excluded from this classification.\*\*

\*This is also called “pink” noise (in contrast to “white” noise) because the lower-frequency components have higher amplitudes. The noise power is distributed uniformly with respect to the log of frequency, whereas with “white noise” (either Johnson or shot noise), noise power is distributed uniformly with frequency.

\*\*A significant component of drift may result from rectified and filtered radio frequency pick-up.

reckoned\* at an appropriate frequency exceeds this resistance, the noise-current source associated with that input terminal will dominate.

If not, the noise-voltage source will be dominant. The “noise factor” for an operational amplifier circuit, for a certain frequency band, is defined as the ratio of the total noise power in that band (as measured at the output of the amplifier) to the theoretical noise power that would be contributed by an ideal resistor equal to the real part of the terminal impedance. It is always greater than unity. Minimum noise factor is obtained when the equivalent resistive component of the terminal impedance equals  $R_s$ , the characteristic noise resistance.

The “noise figure” is defined as the noise factor, expressed in decibels—that is: (Noise Figure) =  $10 \log_{10}$  (Noise Factor). See I.52 for definition of “noise gain”, and for sample noise calculations.

\*This parallel combination of impedances is called the “terminal” impedance of the circuit at the frequency at which it is calculated.

I.9  
I.7  
I.19  
to  
I.24

I.10  
I.7  
I.9  
I.14  
I.50



**I.11 THE NATURE OF DRIFT.** What is this thing called drift? For our purposes, it may be considered to be a gradually-developing change in the offset voltage and both offset currents of an Operational Amplifier. This change in offsets, current or voltage or both, corresponds, in a feedback circuit, to a change in the “null” voltage or current, and is therefore a first-order error. No necessary relationship exists between voltage drift and current drift, not even in regard to polarity. Of course, one may relate a component of each to the amplifier input impedance, but it frequently turns out to be an insignificant component. Drift is also classifiable simply as the bottom-most range in the near-infinite spectrum of “noise”, as noted in I.10.

Prolonged tests of models drawn from our regular production of solid-state amplifiers show that, at room temperature at least, the long-term drift over many

months averages close to zero; certainly it does not show any steady progression or systematic pattern. However, one can with equal certainty expect random fluctuations weekly, daily, hourly, per minute, per second, etc. Whether or not they are appreciable depends, of course, upon the amplifier design and its application. Quite often, though, the “apparent stability” of an amplifier depends, not on random, internally-generated changes, but on the external influences brought to bear on the circuit by environmental and (external) circuit factors,—most notably: temperature, humidity, contamination (of insulation), external-component parameter changes, and power-supply changes. None of these is a true drift factor; all are “stability” factors for the complete circuit. Because apparent drift due to temperature instability is generated internally, as is random drift, it is usually included in the drift specifications of an amplifier.

**I.12 METHODS OF MINIMIZING DRIFT.** We have noted that drift is especially influenced by temperature; to separate this dependency from other influences, it has become customary to rate amplifiers in terms of the maximum change in offset (null) voltage observable over a given temperature range. Drifts with time, at a fixed temperature, are also specified—see the typical specifications, to the right, for typical unstabilized, and stabilized amplifiers.

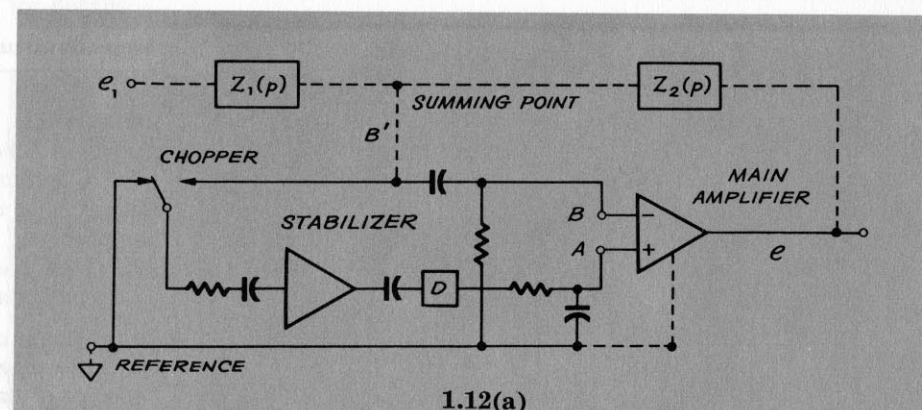
The most effective means of minimizing drift is the use of a modulated-carrier or “chopper” amplifier in the “DC” and low-frequency signal path only. This preamplifier is employed to maintain the effective offset at the negative input terminal as near zero as possible; for this reason, it is called the “stabilizer”.

Chopper-stabilized amplifiers take advantage of the fact that the offset, drift, and noise levels of a narrow-band chopper-modulator/demodulator DC amplifier are 1 to 3 orders of magnitude lower than those achievable in a conventional unstabilized wide-band differential amplifier. By combining the two types, the advantages of both are realized.

The circuit shown here is representative of almost all Philbrick chopper-stabilized Operational Amplifiers. The input signal is connected to two amplifiers: *directly* (DC coupling) to a chopper-modulated/demodulated (slow, narrow-band) stabilizing amplifier; and through a capacitor (AC coupling) to the main (fast, wide-band) amplifier. By careful design, the low-frequency roll-off of the AC path is made to complement the high-frequency roll-off of the DC path. (See I.17.)

A useful way of thinking about the function of the stabilizer is to say that, regardless of the offset generated in the main amplifier, and regardless of the configuration of the input and feedback networks, the stabilizer operates to drive the effective offset at the input terminal ( $B'$ ) to zero, and hold it there. It does this by introducing a DC voltage very nearly equal to the effective voltage offset of the main amplifier into its positive terminal.

The residual offset, as measured at  $B'$ , consists of the inherent offset of the stabilizer (very low... less than 10 microvolts) plus the main-amplifier offset divided by the gain of the stabilizer.



1.12(a)

#### TYPICAL DRIFT SPECIFICATIONS

Input voltage offset:	UNSTABILIZED	STABILIZED	MODULATOR TYPE
Adjustment	Built-in	External	Built-in
vs. temp. ( $-25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ )	2 millivolts	20 $\mu\text{V}$	Not Rated
vs. temp. ( $+10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$ )	0.5 millivolt	5 $\mu\text{V}$	3 mV
vs. time (per day) typical	25 microvolts	<1 $\mu\text{V}$	50 $\mu\text{V}$
vs. time (half hour) typical	10 microvolts	<1 $\mu\text{V}$	5 $\mu\text{V}$
*Narrow-band noise (p-p)	10 microvolts	6 $\mu\text{V}$	1 $\mu\text{V}$
Input current offset (either input)			
+25 $^{\circ}\text{C}$	2 nanoamperes	10 pA	0.5 pA
vs. temp. ( $-25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ )	5 nanoamperes	100 pA	Not Rated
vs. temp. ( $+10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$ )	2 nanoamperes	30 pA	100 pA
vs. time (per day) typical	1 nanoampere	2 pA	0.1 pA
vs. time (half hour) typical	0.1 nanoampere	1 pA	0.01 pA

\*Figures given are for input noise (0.016 Hz to 1.6 Hz).

1.12(b)

I.11  
I.7  
I.12  
I.14  
I.37

I.12  
I.7  
I.11  
I.17  
I.14  
I.37

**I.13 EXTERNAL INFLUENCES.** The degree of freedom from drift and noise achieved in an Analog Circuit depends upon its environment, to a degree often not appreciated. This is particularly true of the more subtle environmental influences, such as the history of humidity exposure and the intensity of radio-frequency pickup.

Temperature is usually the most significant environmental effect. Some amplifiers are remarkably well compensated for steady-state temperature change, but even these show an offset change due to thermal *transients*, and likewise to thermal *gradients* established across the amplifier's interior. Fortunately, it is a simple matter to shield an amplifier from temperature gradients, and almost as simple a matter to insulate it so as to prevent rapid changes (transients) in its temperature.

Humidity can have a significant effect on the components and circuits external to the amplifier, and the beginning Analog Artificer should, before attempting any serious design work, read Sections I.33 through I.36.

**I.14 TOTAL INPUT UNCERTAINTY.** We have now assembled an impressive array of factors—some generated within the amplifier and some introduced by its environment—that contribute to non-ideal input circuit behavior. The ideal input circuit would exhibit infinite input impedances, zero offsets, zero noise (including zero drift) and no pickup or environmental sensitivity. All departures from that ideal may be expressed as *possible* false signal voltages, and as factors of *uncertainty*.

How *much* uncertainty can the application tolerate? The easiest, most conservative, and most expensive answer is obtained by taking

the *worst-case algebraic sum* of all the factors listed, as shown to the right. It is the coward's way, but it may be the way of wisdom . . . and it may not be oppressively wasteful, if second thoughts are not permitted.

The probability of a worst-case departure from zero null is extremely low, however, and it behooves the designer to question the need for algebraically-summed pessimism.\* Further, some factors may not matter much; e.g.,—even low-frequency flicker averages to nearly zero in quite a short time, in a long-term integrator.

\*RMS summing is often an intelligent compromise.

**I.15 FINITE-GAIN ERROR FACTOR.** In I.5 and I.6, we derived ideal response equations, assuming infinite gain and zero null voltage. The assumption that very high gain equals infinite gain is not always justified however; therefore, we must investigate the resulting error. The derivation approach is quite general. Taking as our model an "Inverting Adder", we derive its response *not* for infinite gain but in terms of a *finite gain*,  $A$ , for which the null voltage is:

$$e_n = -\frac{e}{A} \quad (1-6)$$

The resultant response equation is given in Figure 1.15. Its bracketed term is the error factor, which should, ideally, be unity. Note

that the error factor multiplies the expression describing the *ideal* closed-loop relationship. The error factor may be generalized by treating the entire feedback circuit (output to negative input) as a voltage divider of ratio  $\beta^*$ —usually a complex quantity, but shown here, for simplicity, as purely resistive. The feedback circuit so treated should include all parasitic impedances, from whatever source. The general relationship for closed-loop circuits is:

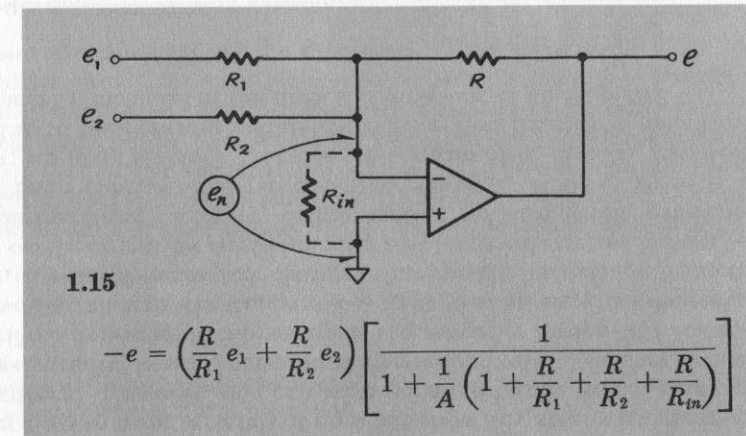
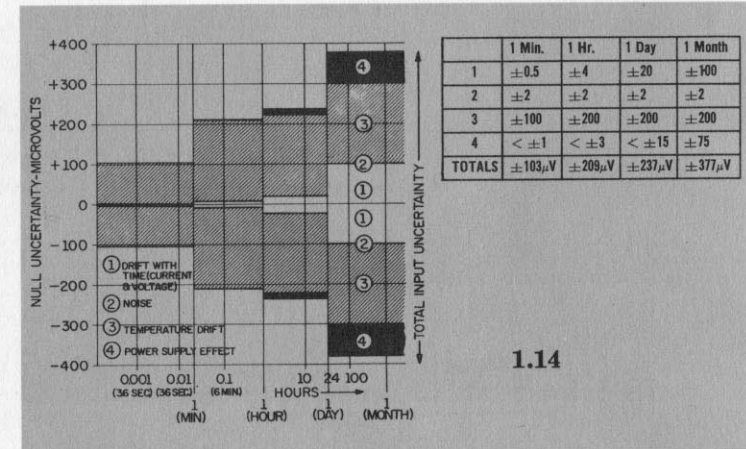
$$-e = \left( \frac{\text{ideal}}{\text{relation}} \right) \left( \frac{1}{1 + \frac{1}{A\beta}} \right) \quad (1-7)$$

\*The "noise gain" referred to in I.52 is  $1/\beta$ .

Radio-frequency pickup can be a stealthy saboteur, plaguing many low-level DC and low-frequency applications. Although its suppression is a well-understood art, its role as a source of drift and low-frequency noise is often overlooked. A well-designed input stage may be expected to be a poor RF detector, but even so it may convert millivolts of RFI into microvolts of DC voltage offset. Modulation of the RF may produce "flicker," hum, and other noise effects. Power lines are notorious as sources of RFI, but even casually-applied test instruments can do great harm—greater, perhaps, for being less often suspected.

All Philbrick Operational Amplifiers have been rendered at least insensitive, if not immune, to humidity, thermal transients and gradients, and corrosive atmospheres—to a degree consistent with the performance class of the Amplifier.

(See I.37).



$$-e = \left( \frac{R}{R_1} e_1 + \frac{R}{R_2} e_2 \right) \left[ \frac{1}{1 + \frac{1}{A} \left( 1 + \frac{R}{R_1} + \frac{R}{R_2} + \frac{R}{R_{in}} \right)} \right]$$



**I.16 COMMON-MODE ERROR.** We now restate equation (1-1), for an ideal differential amplifier, giving the ideal response to inputs  $e_A$  and  $e_B$ :

$$-e_n = (e_A - e_B) = \frac{e}{A} \quad (1-8)$$

where  $A$  is the voltage gain of the amplifier. In section I.4, we also noted that practical differential amplifiers do *not* perfectly reject common-mode signals; i.e., they do *not* respond only to differential signals. We shall now describe Common-Mode Error more explicitly, as an apparent error in the null voltage  $e_n$ , which error may be considered to be in series with one of the inputs, and may be attributed, for the sake of simplicity, to imperfection in the symmetry of the input circuitry.

This imperfection is depicted to the right, with the factor  $CMRR^*$  introduced to express the degree to which the Common-Mode Voltage is rejected. We may now write a more practical expression for the response of a differential operational amplifier: ( $e_{CM} \equiv e_A$ )

$$e_n = e_B - e_A = \left( -\frac{e}{A} + \frac{e_{CM}}{CMRR} \right) \quad (1-9)$$

In practical amplifiers,  $CMRR$  is very high, usually higher than the rated low-frequency, open-loop, full-load voltage-gain,  $A$ . Common-Mode-Rejection Ratios of 20,000:1 to 200,000:1 are easily attainable, even in the presence of many volts of Common-Mode Voltage. Common-Mode Rejection is often expressed in a logarithmic form:

$$CMR = 20 \log_{10} |CMRR| \quad (1-11)$$

In practical differential amplifier applications both accuracy and precision may be limited by both  $A$  and  $CMRR$ ; and in critical applications the effects of both should be considered.

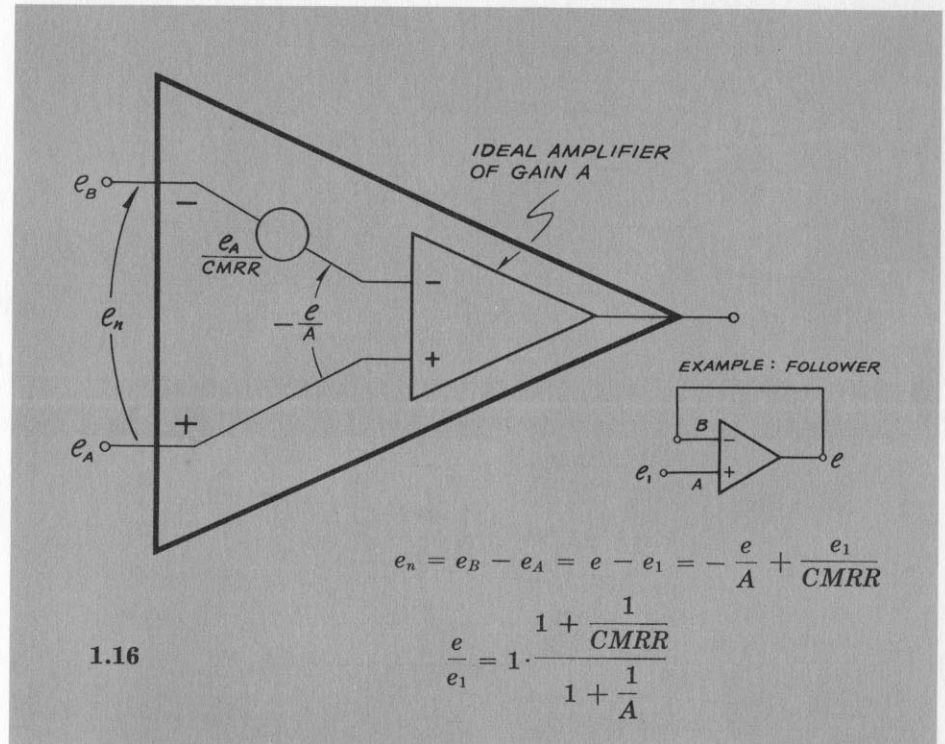
It is important to note that in any given amplifier, the common mode error may vary with frequency, or with the common mode voltage level (i.e., the common mode error is not necessarily linear with input-signal level).

Another possible source of Common-Mode Error is unequal source impedance; if the impedances of the signal sources or the inputs themselves at both inputs

are not equal, the loading of  $Z_{AG}$  and  $Z_{BG}$  may cause apparent  $CME$ ; however, if  $Z_{AG}$  and  $Z_{BG}$  are very much higher than the signal source impedance, this effect is negligible.

The effect of Common-Mode Error on circuit performance is mentioned in many places in this text. It should be noted that it effectively *disappears* whenever either input voltage becomes zero, as when terminal  $A$  is grounded.

It is interesting to note that, with few exceptions, the stability of the operating point (zero-adjustment, for example) of a differential amplifier is measurable in the same terms, and has the same order of magnitude, as the  $CMRR$ . See I.29 for details.



I.16  
I.4  
I.7  
I.29  
I.48

\*Defined operationally in section I.48.

**I.17 OPEN-LOOP GAIN vs FREQUENCY and PHASE-SHIFT.\*** In I.1, we touched on this subject briefly, noting that Operational Amplifiers have a very high open-loop gain at and near DC, and are designed to exhibit an essentially uniform (linear) roll-off of gain with frequency, at the rate of about 6 db per octave† (20 db per decade) starting at a very low frequency. (In other words, they are very definitely *not* designed for a uniform response up to a “cutoff” frequency, followed by a rapid fall-off in gain with frequency accompanied by a catastrophically rapid increase of phase shift, as are so-called “broad-band” amplifiers.) This characteristic, plotted on a log-log scale, is shown to the right. Note that in some amplifiers, notably those in which an auxiliary chopper/demodulator amplifier is used for stabilization against drift, there is a slight “jog” to the characteristic, in the vicinity of the crossover between the AC-coupled and DC-coupled input networks. This anomaly generally has no practical significance.

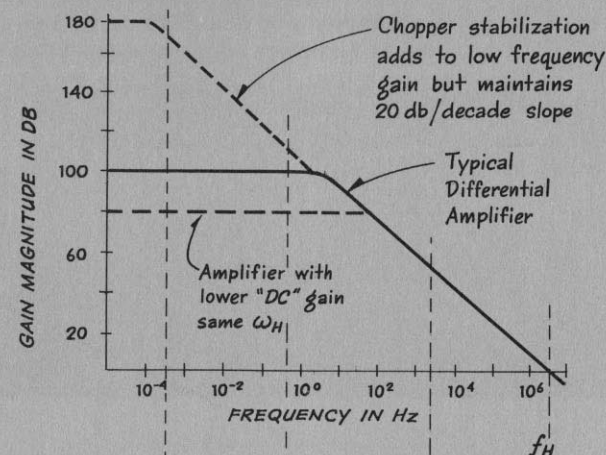
The roll-off curve passes through unity gain at some frequency,  $f_H$ , and continues down, to gain values less than unity.  $f_H$  is often expressed in terms of its equivalent *radian* frequency,  $\omega_H = 2\pi f_H$ . If the log gain vs log frequency curve were a straight line, the amplifier would have a constant gain-bandwidth product, which would then, incidentally, be equal to  $f_H$ , in Hz, since the gain is unity at  $f_H$ .

The phase shift introduced by an Operational Amplifier should be nearly zero in the DC-low-frequency region, and should increase (in the frequency region in which roll-off begins) to a lagging  $90^\circ$ , and stay constant at or very near  $90^\circ$  until the neighborhood of  $f_H$  is reached. In practice, as can be seen from the graph of figure (b), additional lagging phase-shifts, chiefly due to “strays,” are gradually introduced at high frequencies, until, at  $f_H$ , the phase shift is beginning to differ significantly from  $90^\circ$ .

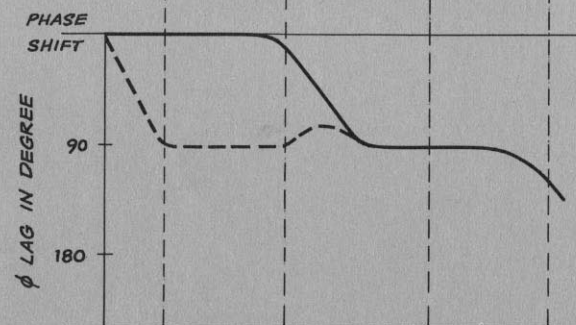
Why are we concerned with the open-loop gain characteristic? After all, the feedback circuit will have a profound effect on the behavior of the amplifier, and it has not yet been mentioned. Further, most applications require appreciable closed-loop gain over bandwidths of only a few kHz . . . why all the concern about what happens above those frequencies? The answer lies in the fact that the Operational Amplifier, like all energy amplification devices, possesses the ability and inclination to oscillate under appropriate feedback conditions. Moreover, because its principal usefulness is almost always realized with large amounts of negative feedback, it is constantly living within the shadow of oscillation.

Nevertheless, if the amplifier is well-designed, there need be no cause for dismay. However, in order for a *practical* universal Operational Amplifier to be stabilizable by explicit methods under all conditions of resistive feedback, its open-loop gain characteristic should (indeed, it *must*) conform to the description given above . . . as do nearly all Philbrick Amplifiers but certain special-purpose types, the unique strengths of which lie elsewhere. A full discussion of the techniques recommended for achieving dynamic stability is given in I.44.

1.17(a)



1.17(b)



Note that the amplifiers for which our curves are drawn have nearly *constant gain-bandwidth products*.

\*In this section we define small-signal behavior and ignore rate-limiting effects. For sinusoidal output, the maximum amplitude-frequency product is related to the maximum slewing rate by

$$(\omega E)_{\max} = \left| \frac{de}{dt} \right|_{\max}$$

Typically, the maximum frequency at which full-scale output can be achieved is 100 to 200 times smaller than  $f_H$ .

†  $-6.02 \text{ db} = 20 \log_{10} \left( \frac{1}{2} \right)$ , or gain is reduced by 2:1 for each doubling of frequency.

I.17  
I.7  
I.15  
I.37  
I.42  
I.43  
I.46  
I.47



**I.18 OTHER IMPORTANT REALITIES.** This group of Operational Amplifier non-idealities have this in common: either they are as difficult to control as the foregoing Departures from the Ideal (I.7–I.17) but plague us far less frequently; or, conversely, they are almost always with us, but are easily controlled.

● **NON-LINEARITIES.** The output, input, and gain characteristics all exhibit non-linearity. Fortunately, in most applications within ratings, these non-linearities are negligible.\* There is both input and output voltage saturation—the inability to accept or deliver more than a certain peak-to-peak signal. Often, the positive and negative saturation limits are symmetrical around zero. In general (but not always) the output circuit saturates earlier, unless the gain falls quite low.

Then there is output current saturation, at and below some limiting value of load impedance, *before* the amplifier reaches nominal voltage saturation. (The load includes the feedback circuit.) The output voltage swing and the linear current swing are interdependent, as shown in (a).

Figure (b) shows the significance of amplifier non-linearity when circuit gain is high (i.e., with “loose” feedback:  $R \gg R_1$ ). The output deviates from that dictated by  $e_{in}$  by  $(e_{in} - e_n)$ , where  $e_n$  is  $-e/A$ . For looser feedback, i.e., at high noise gains  $e_n$  is larger, in relation to a given input, and the distortion is greater. For “tighter” feedback, (e.g.,  $R = R_1$ )  $e_n$  is so small relative to  $e_{in}$  that amplifier non-linearity is negligible.

Finally, non-linear behavior in any part of an amplifier circuit may combine with the inherent rolloff characteristic of the amplifier to cause very significant differences between the small-signal and large-signal transient-response characteristics. Because this effect limits the maximum “slewing-rate” (the rate at which the output will move between full-scale negative and full-scale positive) it is called “Rate Limiting.” (Apparent Rate Limiting may also occur if, when driving large capacitive loads, the amplifier current ratings are exceeded.)

● **INPUT-IMPEDANCE LOADING.** The specified input impedances of an Operational Amplifier are not ideally infinite, although they may be very high compared to the external circuit parameters chosen. The common-mode impedances,  $Z_{AG}$  and  $Z_{BG}$ , are generally far higher than the differential impedance,  $Z_{AB}$ . Usually  $Z_{AG}$  and  $Z_{BG}$  are high enough, and well-enough matched, so that unsymmetrical source regulation (a source of common-mode error—see I.16) is negligible—but not always. See figure 1.18(c).

The impedance values given in specification charts are always *dynamic*, *small-signal* values, and always *minimum* or *nominal* values. Input impedances may be a function of the common-mode (i.e., may be non-linear); hence, they may contribute to non-linear response, unless their effect is minimized by careful selection of the amplifier and external-circuit parameters. In the Adder-Subtractor of II.5, for example,  $Z_{BG}$  and  $Z_{AG}$  load the summing points, and *may* be significant; in the Unity-Gain Inverter of II.1,  $Z_{AB}$  (in parallel with  $Z_{BG}$ ) loads the summing point, and *may* matter; in the Follower of II.2, however,  $Z_{AB}$  and  $Z_{BG}$  are driven from the (very low) output impedance, and are usually unimportant, whereas  $Z_{AG}$  is the principal component of the input impedance.

● **SHUNT CAPACITANCE AT THE INPUT.** One of the assumptions made about ideal circuits (I.5–I.6) was that they were *stable* . . . that is, that they did not oscillate or exhibit “ringing” in response to transients. Stability is discussed in detail in I.42, but note for now that the feedback circuit must not contribute

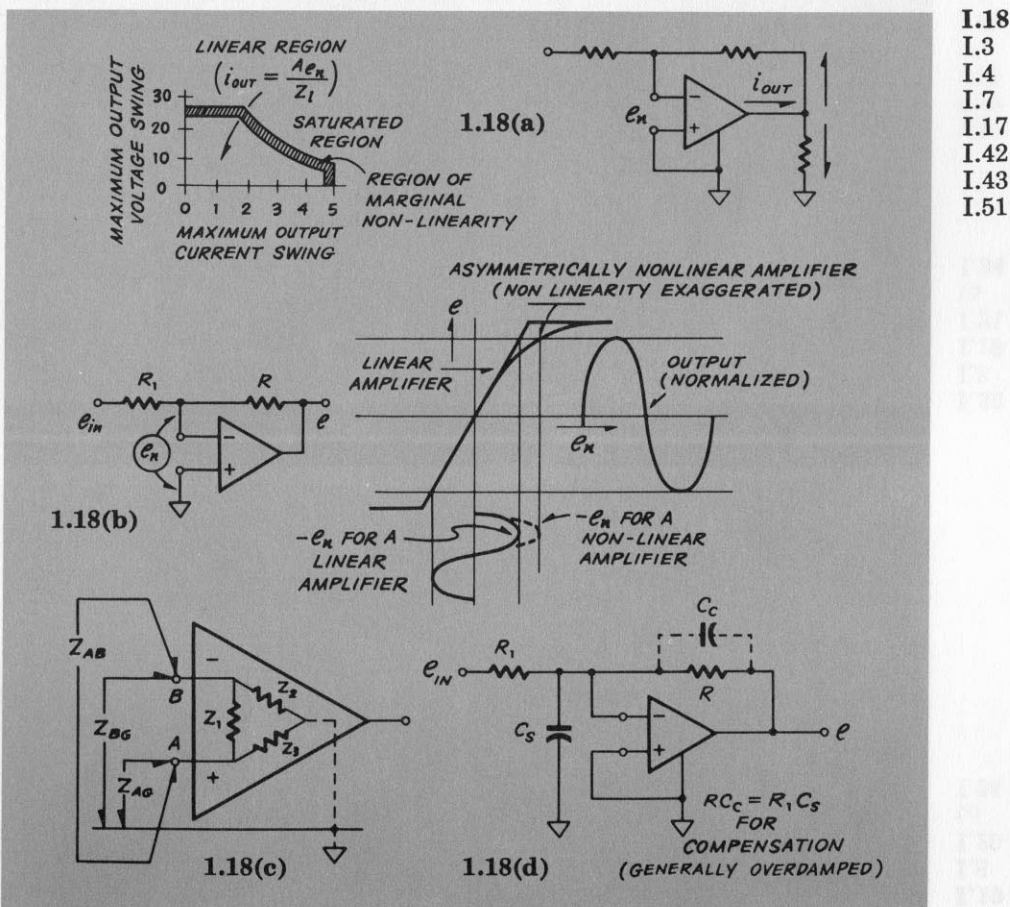
significant phase shift to the loop. In (d), we have introduced, for the first time, the shunt capacitance,  $C_s$ , that loads the summing junction. Even with careful wiring, at least 10–20 pF is inevitable; and, with feedback resistors of the order of megohms, this can cause instability, even with modest-gain-bandwidth-product amplifiers.

Fortunately, it is only necessary to add a small compensating capacitor,  $C_c$ , having a value, typically, of:

$$C_c = \frac{R_1 C_s}{R} \quad (1-12)$$

If very fast response is not required, (1-12) yields a good value. Often, a considerably higher capacitance is installed, to curtail unwanted noise and bandwidth (see I.52); but if broad bandwidth is required, excellent stability can usually be obtained with a much *smaller* capacitor than equation (1-12) would indicate. In any case, a feedback capacitor is *always* in order, and the higher the capacitance the circuit can afford, the better.

\*For several good reasons we often deliberately introduce non-linearities into the feedback circuit to affect the output performance characteristic—see I.25—or into the input circuit—see I.27.

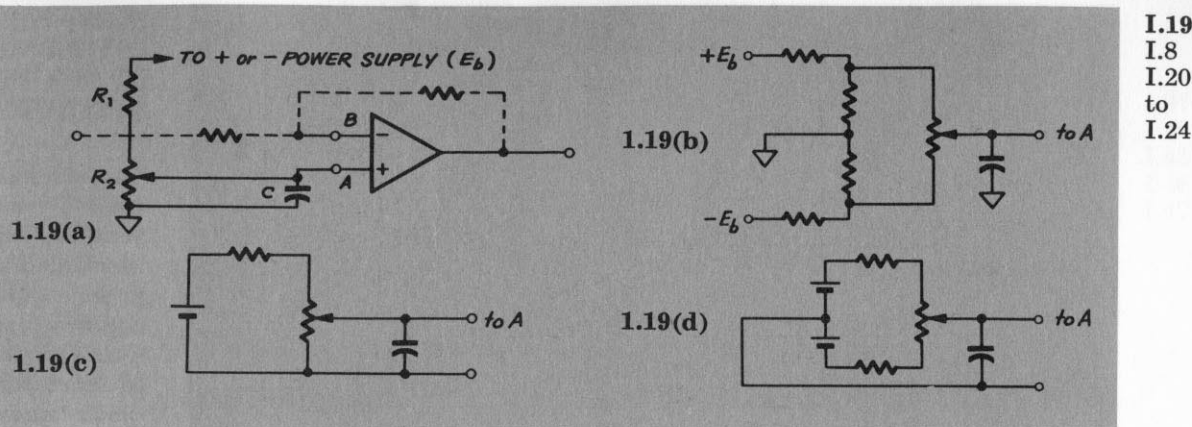


I.18  
I.3  
I.4  
I.7  
I.17  
I.42  
I.43  
I.51

**I.19 EXTERNAL VOLTAGE BIAS.** All Philbrick solid-state Operational Amplifiers have either special terminals for external adjusting circuits, or built-in adjustment, the purpose of both being to achieve zero voltage offset. The internal adjustments, or the recommended external adjusting circuit when provided, should be used in preference to those shown here, to minimize temperature drift and assure proper internal operating points.

Circuits (a) and (b) may be used at the positive input of a single-ended amplifier, (b) providing bipolar adjustment. Circuits (c) and (d), since they use cells, may be useful in differential amplifier applications, in which the bias supply must often "float."

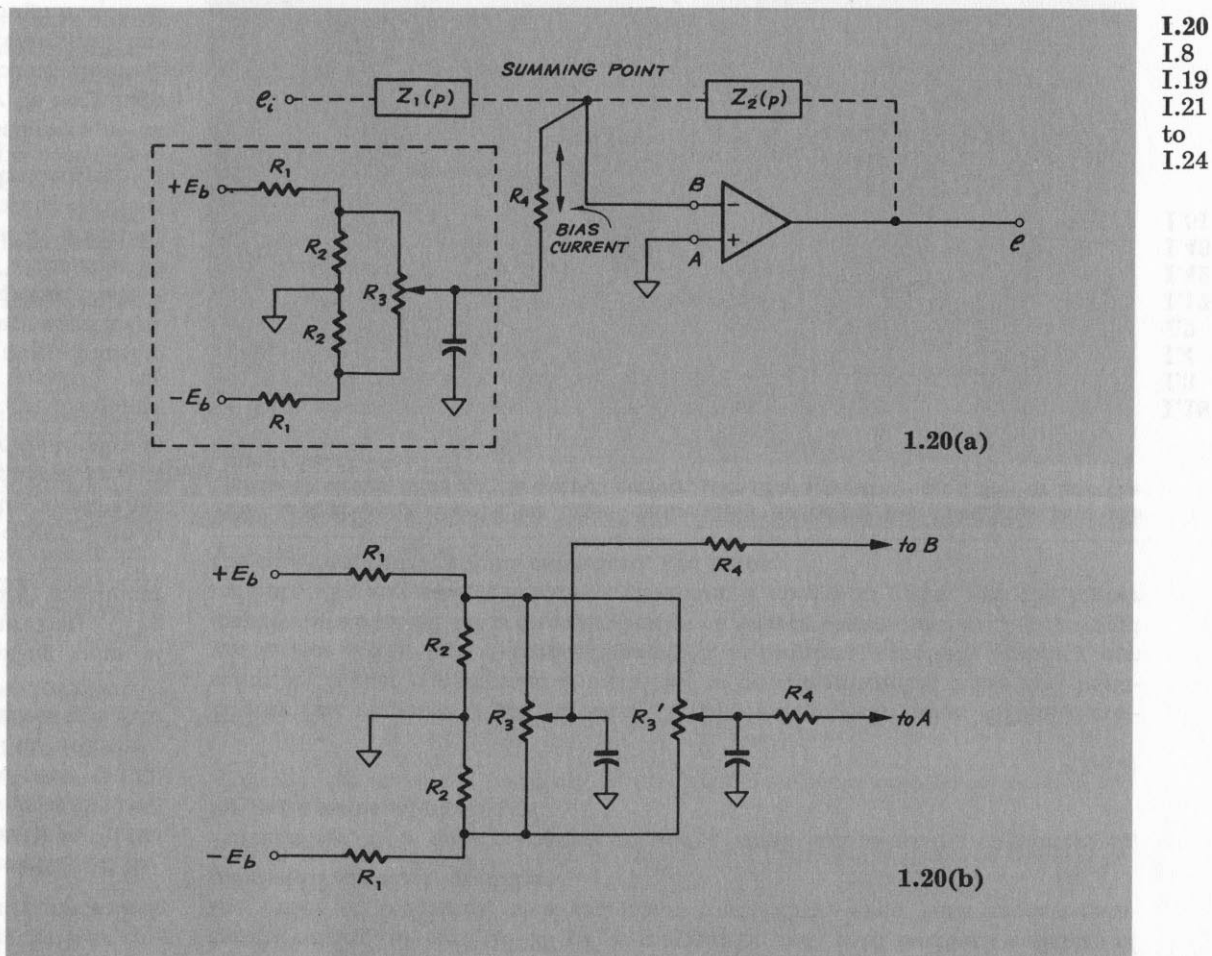
Care should be exercised in component selection for all bias circuits, since drift in them will give rise to apparent amplifier drift.



**I.20 EXTERNAL CURRENT BIAS.** Offset currents of either polarity may be supplied to terminal B in circuit (a) through a high resistance,  $R_4$ . (It should be noted that the  $R_1$ - $R_2$ - $R_3$  circuit may be replaced by a potentiometer *only*, provided that the power supply provides a "clean" neutral terminal, for a discussion of which, see I.29 and I.30.)

Note that the part of circuit (a) that is contained within the dashed rectangle is the same as one of the voltage-bias circuits of I.19(b); in fact, *any* of the bias circuits of I.19 may be used to develop current bias\*, but it is less likely that the cell circuits would be used, since a higher voltage across the potentiometer permits the use of a larger value of  $R_4$ .

Circuit (b) may be used\*\* to furnish adjustable, reversible bias currents to *both* inputs, provided either that the summing-point potential remains at or very near ground, or that the bias-supply "center-tap" may be floated and returned to a circuit point that is always at or near the summing-point potential, *or* that the variations in the summing-point potential are small compared to the voltage driving  $R_4$  and  $R_4'$ .



\*In particular, the divider circuit of I.19 (a) is well suited to current biasing of certain amplifiers having known, unipolar current offsets.

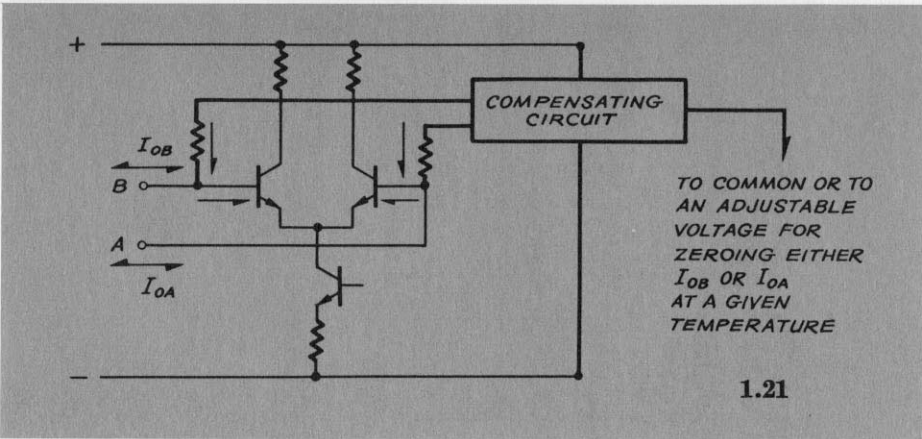
\*\*At some small sacrifice in *CMR*, possibly, if the impedance unbalance introduced by the bias circuit is significant.



**I.21 INTERNAL VOLTAGE & CURRENT BIAS.** In most families of Philbrick Operational Amplifiers, there exist types in which voltage offset adjustments are self-contained. There are also types whose offset adjustment terminals are available, either for remote adjustment or for installation of fixed external resistors, in which bias adjustment is unnecessary or undesirable.

If very-nearly-perfect current biasing must be accomplished, it is usually accomplished externally, by connecting a recommended bias circuit at the amplifier's input terminals. However, there exist "compensated" amplifiers, in which current offsets are reduced to about 20% of the offsets in the prototype design of the family. In several of these types, an external terminal is available, to which a voltage bias may be applied to "zero" the offset current at either input, without loading that input.

The circuit shown at the right has temperature-compensated adjustable current bias, and is typical of compensated ("C"-type) Philbrick amplifiers.



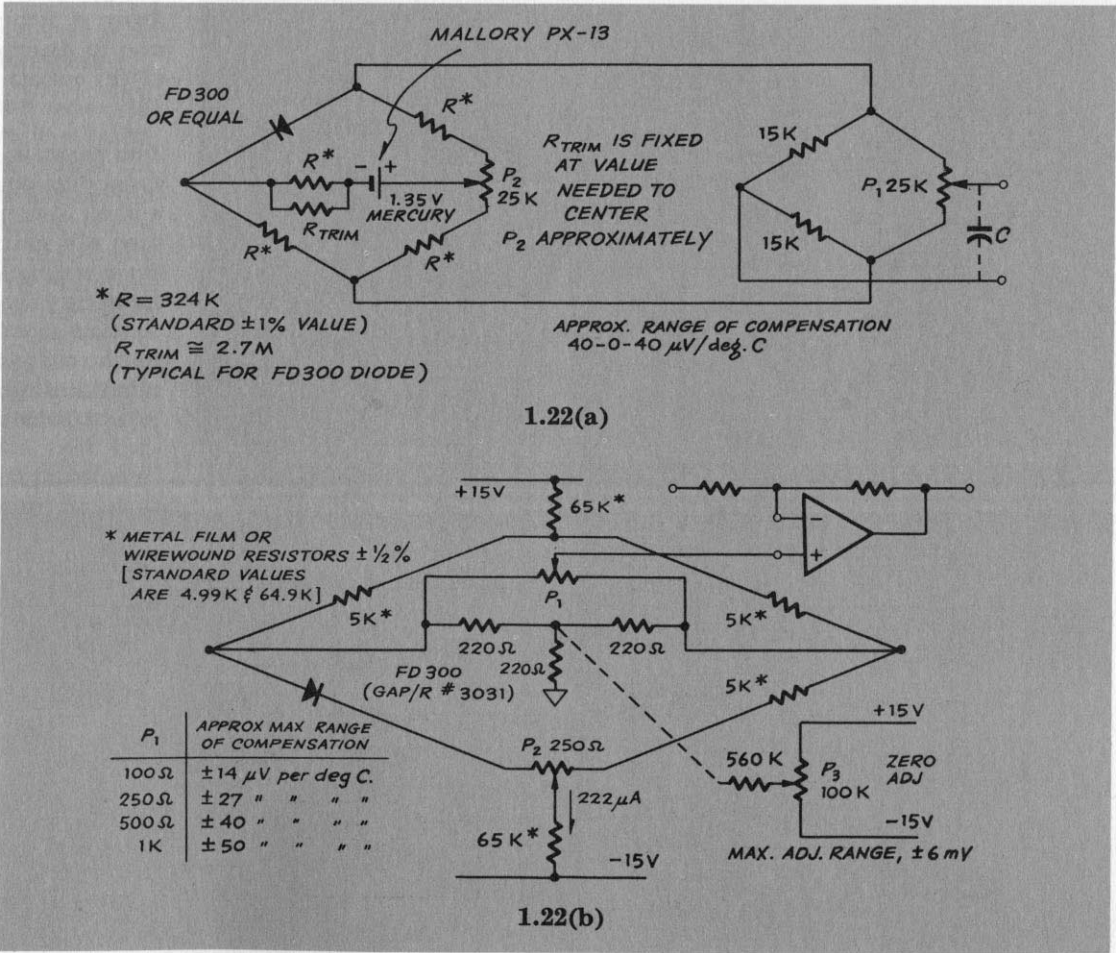
I.21  
I.8  
I.19  
I.20  
I.22  
to  
I.24

**I.22 TEMPERATURE-COMPENSATING BIAS CIRCUITS.** The inexpensive circuit shown in (a) is designed to be inserted in series with either input to an operational amplifier for which bias (zero-adjustment) has already been provided.

First,  $P_2$  is adjusted so that, at room temperature, manipulation of  $P_1$  has no effect, indicating that zero volts must now exist across the 15kΩ bridge. Presumably, at any other temperature, an offset will have developed in the amplifier. By re-zeroing the output, using only  $P_1$ , the entire circuit is exactly zeroed, at least at two temperatures. Because this circuit can be made physically small, its capacitance to ground may be kept low, and it can usually be connected in series with either input (floating). The 50-cent mercury cell recommended should last 15 years.

Figure (b) shows a similar circuit, intended for non-floating use, and operated from the amplifier power supply. First, at room temperature,  $P_2$  is adjusted so that manipulation of  $P_1$  has no effect. At some new temperature, typically toward the extreme of the desired range of operation, the amplifier is re-zeroed, by manipulation of  $P_1$  only. The temperature coefficient of the resistors used in these circuits is unimportant, provided that it is repeatable, but the resistors must be stable with time, humidity, etc. Selective assembly or trimming to accomplish rough balance of the bridges (with  $P_2$  centered) would obviate the need for  $\pm 1/2\%$  tolerances on starred resistors.

Both of these circuits will reduce the effect of a 25°C temperature change to the effect of approximately 1°C change, when used with most Philbrick amplifiers.



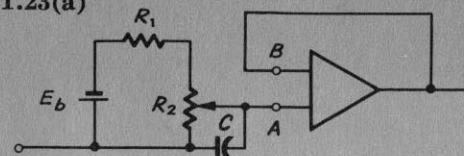
I.22  
I.8  
I.19  
to  
I.21  
I.23  
I.24

**1.23 FOLLOWER BIAS CIRCUITS.** Here are some biasing methods for use when Operational Amplifiers are used as voltage followers (see II.2). Circuit (a) has high input impedance with no attenuation, but has the capacitance of the bias circuit shunted across the input. Circuit (b) also provides high input impedance, but transfers the shunt capacitance to the low-impedance output. Both are unnecessary in amplifiers having internal voltage bias.

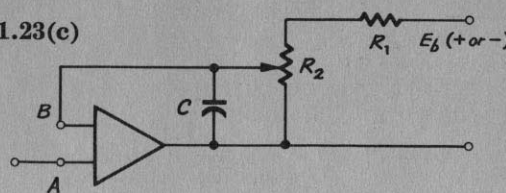
In (c), no cell is required, but the follower is left with a gain slightly higher than unity, due to the attenuation of feedback (see II.2). This can be avoided by using a constant-current source in place of  $R_1$ .

In (d) we show a scheme for *current* biasing.  $R_3$  is very high—perhaps  $10^7$ – $10^9 \Omega$ —and lowers the input impedance only slightly.

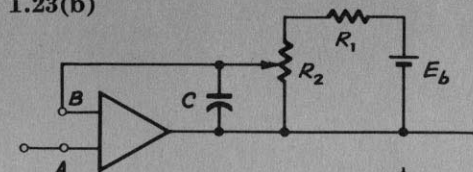
1.23(a)



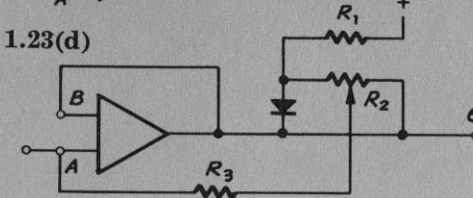
1.23(c)



1.23(b)



1.23(d)



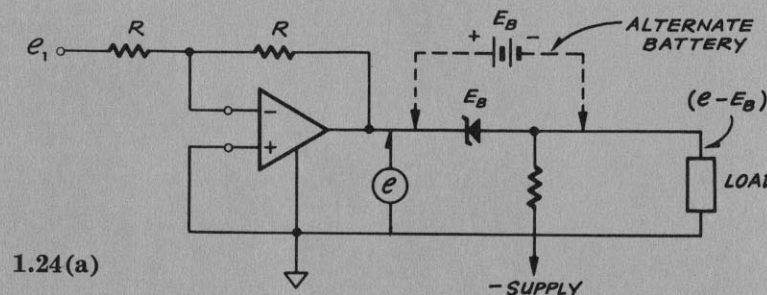
I.23  
I.8  
I.19  
to  
I.22  
I.24

**1.24 BIASING THE OUTPUT VOLTAGE.** Sometimes it is necessary, or at least convenient, to develop the output signal,  $e$ , around an operating point other than zero. This is not at all difficult when the bias-plus-range of the output is still within the output range of the amplifier—in summing-amplifier circuits, one simply supplies an additive bias having appropriate scale factor as an input signal. However, it is not well known that, so long as the *range of output swing* (due to signals) and the maximum required value of output current are both within the amplifier's ratings, the output of the amplifier circuit may have a precise initial setting at a value of voltage many times that of the amplifier's maximum rating, *without using a booster*. The practical technology involved may be worth discussion.

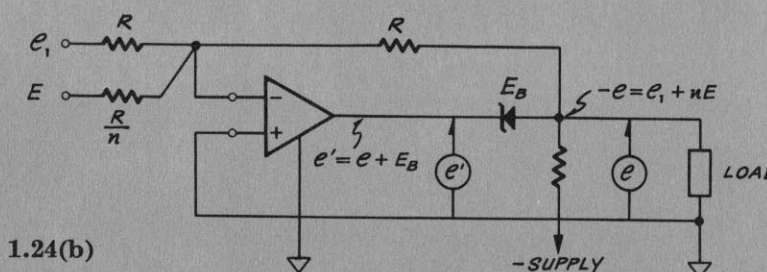
First, an approximate approach: In the unity-gain inverter of circuit (a), a battery or zener diode,  $E_B$ , is used to bias the output. Either polarity of bias may be used; we show a negative operating point here. This circuit is easily realized, but drift in the battery or in the zener voltage could cause significant error, since it would be external to the feedback loop. If the load impedance is low, the zener or battery impedance will also cause a loss in gain.

Circuit (b) is better. The feedback is connected around  $E_B$ , effectively eliminating its drift, and the *dynamic* performance is unaffected by the presence of the zener; that is, the circuit provides an output precisely determined by the inputs and the feedback network, and the sole function of  $E_B$  is to maintain the amplifier output within the amplifier's working range. As an example of this, assume that the normal rated output voltage range of the amplifier is  $\pm 10$  V, and that  $E_B = 10$  V. The amplifier will then function as a precise unity-gain inverter for total effective inputs of 0 to  $+20$  V, producing outputs ( $e$ ) of 0 to  $-20$  V... while  $e'$ , the unbiased output, is varying from *approximately*  $+10$  to  $-10$  V.

Note: Be sure amplifier can supply worst-case output current at all levels.



1.24(a)



1.24(b)

choose  $E_B \cong nE$ , if  $e_1$  has symmetrical positive and negative amplitudes.

NOTE: be sure amplifier can supply worst case output current at all levels.

I.24  
I.19  
to  
I.24



**I.25 BOUND CIRCUITS—WHY & HOW.** “Bounding” means restriction of the output voltage to some assigned maximum, even when the input signal exceeds its assigned full-scale value (either polarity). In practice, this is generally accomplished by use of a supplementary and non-linear feedback circuit, such as those shown here. Note that the ideal “bound” circuit is *dormant* until full scale is reached, at which time it takes over the job of supplying the feedback current necessary to balance the loop, at no significant increase in  $e$ .

So far as the amplifier is concerned, the output voltage *could* be restrained by a non-linear load, such as a zener diode connected across the normal load, or it could be allowed to go to its own limit, probably without permanent damage.

However, after an amplifier “saturates”, i.e., has gone off to a limit, it can require many seconds—even minutes—before it recovers its former zero adjustment.† This is particularly true of chopper-stabilized designs. (The time required for the actual recovery of the zero setting, to within, say, the typical value of short-term drift, may well take 10,000 times as long as the “recovery time-constant” often quoted for an amplifier.)

The use of “bound” circuits effectively eliminates the problem of recovery from overload by *preventing* both the occurrence of overload and its consequences.

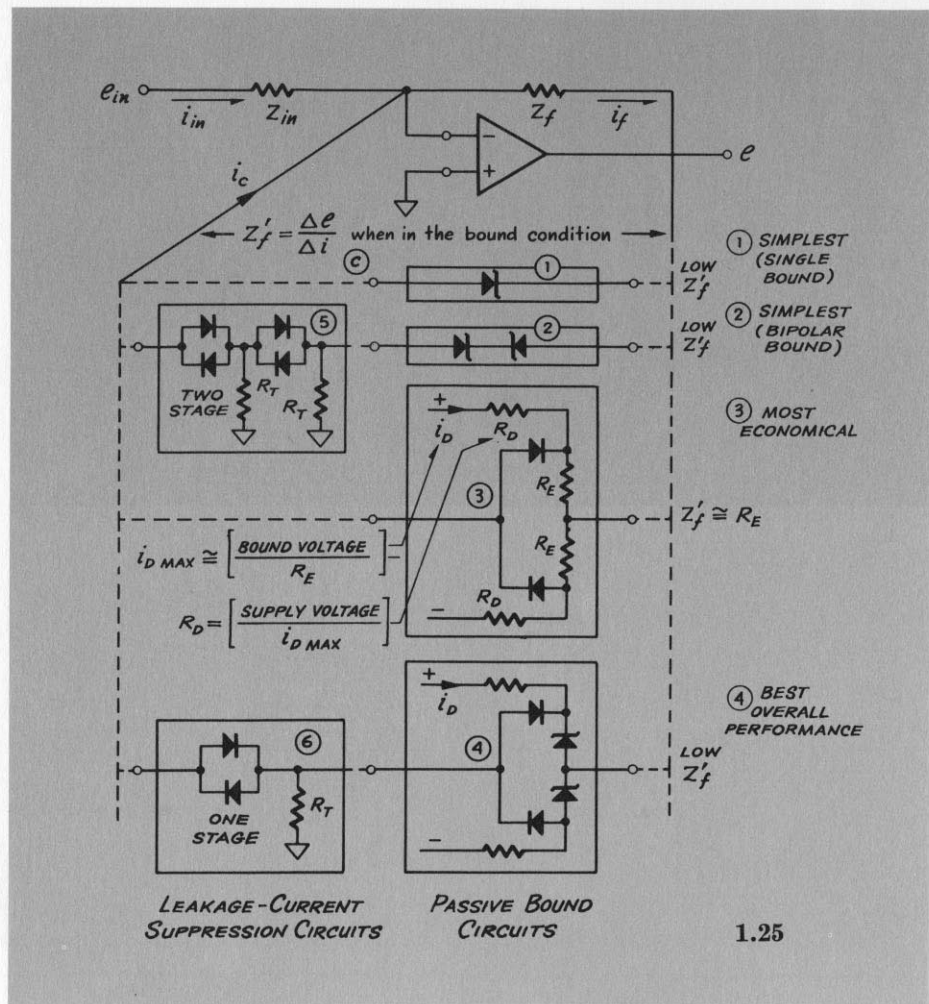
The ideal bound circuit would have an infinite “dormant” impedance *below* the critical value of bound signal, and zero “active” impedance above that value . . . in fact, it would resemble in those respects an ideal zener diode. Since, for almost all applications, both upper and lower bound limits must be established (i.e., both positive-going and negative-going signals must be limited) a pair of such ideal zener diodes would have to be used in the bound circuit. Since most applications specify symmetrical bound limits, we usually strive to make the voltage at which the bound circuit begins to conduct the same for the upper bound as it is for the lower bound.

In practice, the performance we have just described is approached with varying degrees of fidelity by circuits that range from simple to complex, and from inexpensive to quite costly, with performance roughly related to the cost and complexity invested. In the diagram to the right, we have shown and annotated some practical bound circuits, about which the following brief comments may be instructive:

- The simple zener bounds of circuits (1) and (2) frequently have need of leakage-current decoupling; for example, by means of diode-resistor Tee networks\*, such as (5) and (6). This is especially true if  $i_c$  must be minimized.
- If  $Z'_f$  must be very low in the “active” mode, the zener bound is the preferred

†Non-chopper-stabilized types will recover to within thermal-offset range in well under one millisecond after even prolonged overload.

\*See I.26 for a more complete discussion of the Tee network. The decouplers shown in (5) and (6) are extensions of the resistive Tee, wherein diodes are used to achieve thresholds.

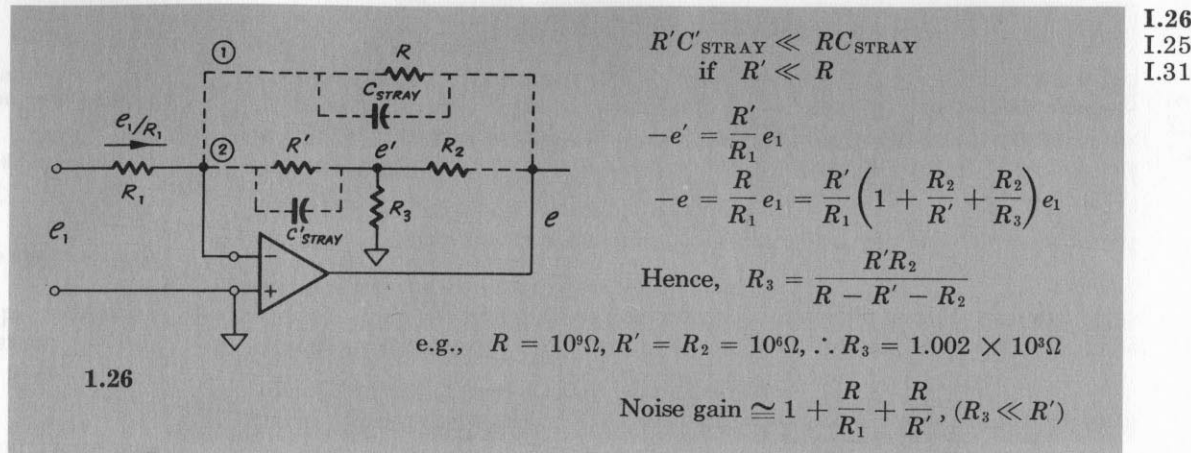


circuit. This is especially the case when the allowable excursion in  $e$  (when bounded) must be held to very small values.

- In designing decoupling circuits, such as (5) or (6), select diodes that have relatively high forward drop at about a microampere of forward current. This will enhance the isolation effect of the Tee.
- Shielding and guarding the low-potential terminals of the Tee may be required to achieve *extremely* low dormant-mode leakage.
- Circuits (3) and (4) have less reverse leakage than (1) and (2), but circuit (3) allows a greater excursion in  $e$  in the “active” mode, and circuit (4) is the most expensive. The combination of (4) and (6) has superb characteristics; (4) and (5) combine to approach the ideal; (2) and (5) approach the ideal at low voltage.

**I.26 TEE NETWORKS.** It is often desirable (and sometimes necessary) to replace a large feedback resistor by a 3-terminal resistance network, so proportioned that it has the same feedback effect, but higher accuracy, lower cost, and far less susceptibility to stray-leakage and stray-capacitance errors, because the tee network establishes much lower feedback impedance levels, end-to-end and to ground.\* In the figure,  $e'$  must be equal to the product of input current and  $R'$ . This can occur only if  $e$  is equal to the product of  $e'$  and the inverse of the attenuation ratio of the divider formed by  $R_2$  feeding  $R_3$  and  $R'$  in parallel. Hence large values of  $R$  can be simulated by a 3-terminal network using practical values of resistance.

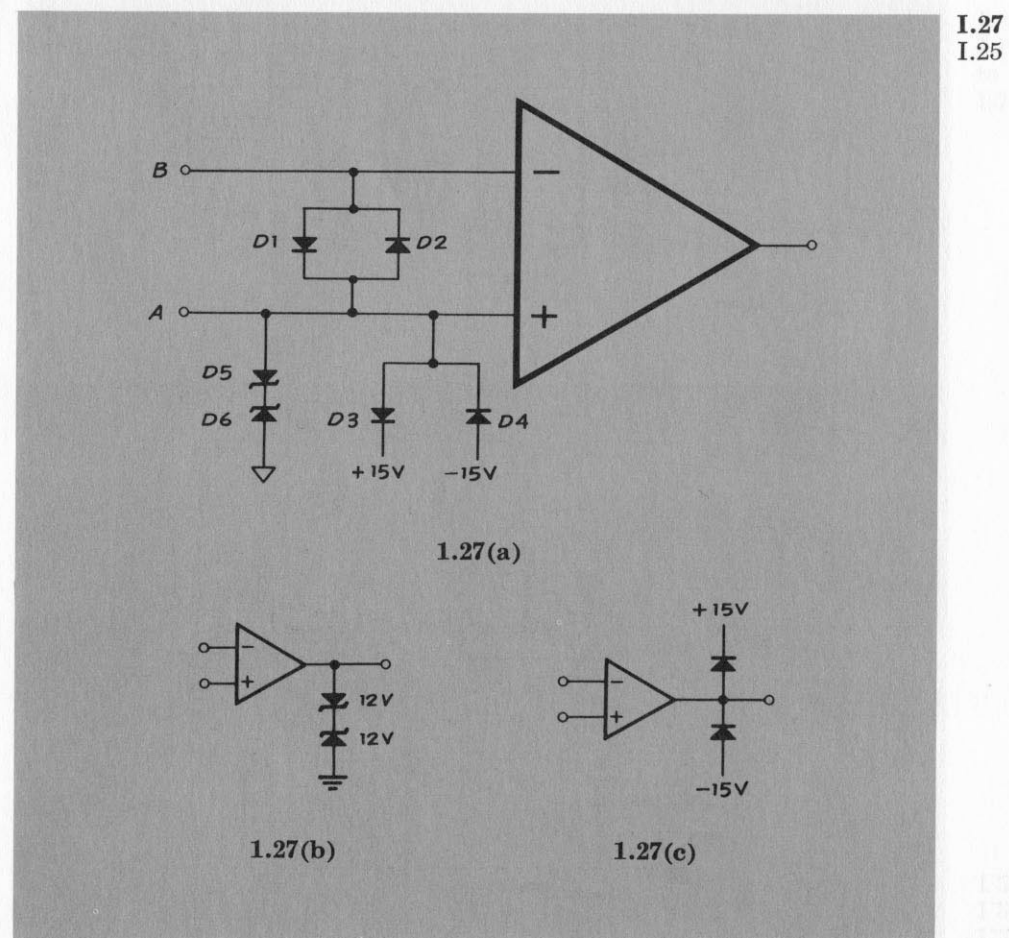
\*We also use nonlinear Tee networks to reduce "dormant" leakage in bound circuits (I.25).



**I.27 FAULT-PROTECTION, INPUT AND OUTPUT.** The bound circuits described in I.25 serve to restrict the excursion of the amplifier output voltage when the input signal exceeds its assigned "full-scale" value. They do not automatically restrict the flow of resulting fault currents within the amplifier to safe values. When very high voltages or currents can exist in the presence of a fault, additional protective measures should be taken.

Automatic limitation of amplifier input voltage can be accomplished as shown in diagram (a) by connection of a pair of diodes  $D_1$ - $D_2$  across the input. In most circuits, a few hundred ohms in series with each active input will not affect accuracy, and will protect the diodes from excessive currents, in the event that a "stiff" voltage supply of excessive magnitude is connected across the input. Protection against excessive common-mode voltage in 10-volt amplifier circuits is obtained by adding an additional pair of diodes to each input, as are  $D_3$  and  $D_4$  biased to positive and negative 15 VDC, as indicated in the diagram, or by a pair of 12-volt ( $\pm 10\%$ ) zener diodes ( $D_5$  and  $D_6$ ) for each input, connected from the input to ground.

Protection of the output circuit against inadvertent load short-circuits is an inherent part of Philbrick amplifier design. Shorting the output to ground does no harm at normal operating temperatures (should be avoided in solid-state units operating above  $65^\circ\text{C}$ ), and shorts to either supply voltage can be tolerated for brief periods. Prolonged shorts should be avoided, particularly in high-output units, to prevent damage to or alteration of component characteristics by excessive heating. A pair of 12-volt zener diodes between output and ground as in diagram (b), or reversed diodes to the  $\pm 15$  VDC supplies in diagram (c) will provide insurance against damage from accidental connection of the output to higher-voltage sources. In all cases, diodes should be low-leakage types, with appropriate current and wattage ratings for worst-case fault conditions.





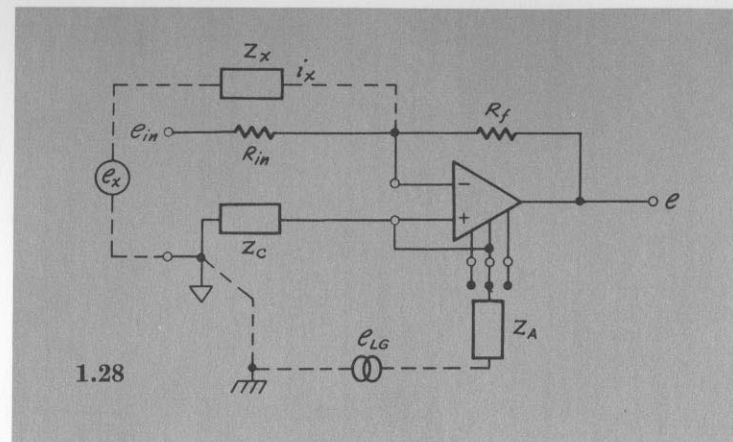
**I.28 THE NEED FOR AN INTERFACE PHILOSOPHY.** In the real and unyielding world of circuits that *work*, we must emulate the best physicians (who treat the *whole* man) and treat the *whole* amplifier, including its complete “circuit environment.”

The innocent circuit drawn in solid lines may be prey to dozens of (curable) ills, two of which are shown in dashed lines. Another malady is shown in 1.29(a). Now then:

- In 1.28, if  $R_{in}$  is 2.0 megohms, and  $e_{in}$  is one volt, how much leakage coupling ( $Z_x$ ) is required from a voltage source (AC or DC) of 100 volts ( $e_x$ ) to produce a noise signal equivalent to 0.1% of the input signal?

*Answer:  $Z_x = 200,000$  megohms. (At 60 Hz AC, just about 0.01 pF will do it!)*

- Again 1.28, if power supply common is coupled to the 60 Hz AC line ( $e_{LG}$ ) with about a megohm ( $Z_A$ ), how much common impedance ( $Z_C$ ) must creep into the grounding connection to produce 1.0  $\mu$ volt more input noise? *Answer: About 10 milliohms. (About 8 inches of #22 wire!)*
- How much current must be returned through the power-common, from the load on amplifier #3, (1.29a) to create a 0.1 mV error between the reference grounds of Amplifier #1 and Amplifier #2, if  $Z_C$  is 50 milliohms? *Answer: Only 2 mA! The cures? Read on!*



I.28  
I.13  
I.29  
I.30  
I.31  
I.39

**I.29 A POWER SUPPLY PHILOSOPHY.** It is a common conception that operational amplifiers are, by nature, extremely tolerant of such power supply misbehavior as regulation, random fluctuations, long-term drift, hum, noise, ripple, and transients; some designers even suggest that an unregulated DC supply is adequate for all but the most critical applications. Though this is to a great extent true, experience—supported by logic—forces us to mention important qualifications.

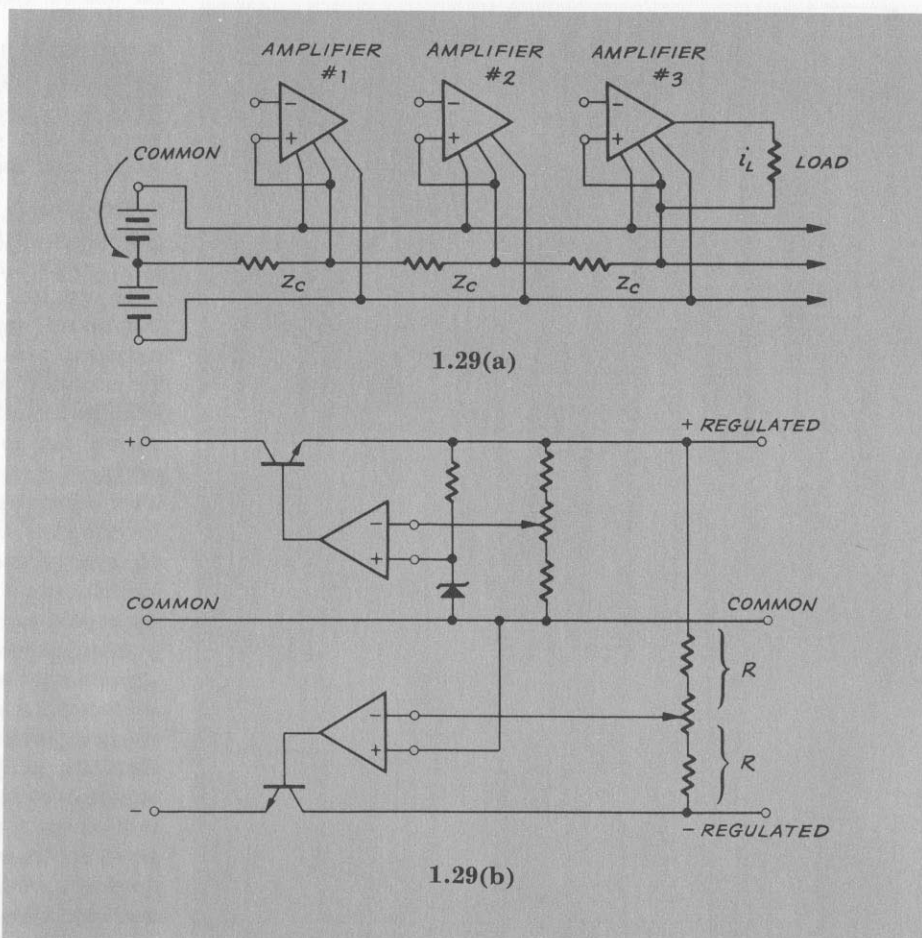
The influence of power supply *regulation and drift* may be small, but it is there; and, even in applications not requiring differential amplification with high CMRR, power-supply voltage variation is a potential source of common-mode error. Good tracking of the positive and negative supply voltages helps reduce it.

Any appreciable *internal impedance* in the supply and its leads provides unwanted coupling between and among amplifiers that share it. See 1.29(a).

Power-supply changes that would go unnoticed if slow—and if used in large-signal circuits, can penetrate to a low-level pre-amplifier stage that is “rate-coupled” to the supply; hence, supply-voltage *transients* may not be ignored.

Hum and ripple are important *noise* components often found in the output circuits of poorly-supplied Operational Amplifiers; “refer” them to the input, if you will, but they probably originate not there, but in the supply . . . and that is where they should be scotched.

For the above reasons, Philbrick power supplies (highly recommended!) are all well-regulated, extremely-well-filtered, low-noise, dual-output designs, with the positive and negative outputs *inter-referenced* (as shown in the 1.29(b) diagram) for good tracking. Anything less than a high-performance supply is a disservice to most designs, and probably poor economy. Is a day of debugging worth an ounce of prevention?



I.29  
I.16  
I.28  
I.30  
I.31  
I.39

### I.30 GROUNDING PHILOSOPHY.

"Ground," in the ideal electronic amplifier, is a single point, common to all input, output, and power circuits. Practical amplifiers exhibit small but finite impedances in circuit returns— $Z_1, Z_2, Z_3, Z_4$  in (a)—and we accordingly designate three distinct grounds: *Chassis Ground*, *Power Common* (the DC-power-supply return), and *Signal Ground*, often designated "high-quality" ground, or simply HQG. Their symbols appear at A, B, and C, respectively. The point C' is the "reference zero," and the object of any intelligent grounding technique is to minimize the potential differences between A, B, C, D, and C'.

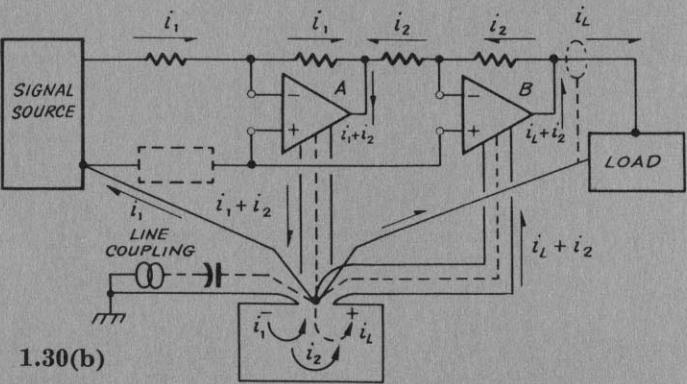
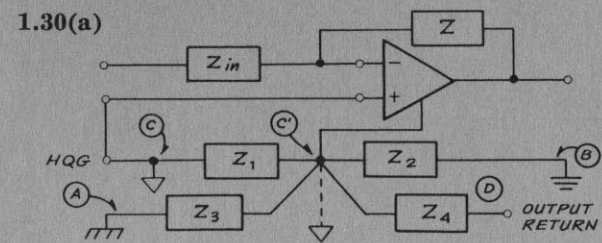
Figure (b) illustrates some recommended practices. First, a floating signal source for amplifier A is grounded to the power common. The amplifier reference inputs (which require insignificant current) may be connected either to power-supply common at the system tie point, or, as shown, to the signal-generator input. The voltage-difference "error" so introduced is only the (small) signal current,  $i_1$ , times the (low) ground-path resistance from signal-source to power supply. To assess its significance, compare the ground-wire and contact resistance with the input resistor of A, since they are in series. It is obvious that this error is probably negligibly small. *Significant* error could however arise if the *load* current,  $i_L$ , were to flow in the lead coupling the amplifier's reference input to signal ground.

Note that amplifiers, computing interconnections do not require ground currents to flow unless ground appears explicitly as a network termination. Also, if either  $\pm 15$  volts is to be used as a reference signal, it is best to run separate reference and power leads back to the supply. When supplying heavy load currents, or when the output contains large, rapid voltage transients, it may be wise to use a twisted or shielded pair. The load should be returned directly to the power-supply common. Multiple-power-supply systems often require that substantial computing current flow in the interconnecting ground bus. This bus should be heavy, short, flat, and highly conductive. Power-line and harmonically-related noise may be caused by insufficient electrostatic isolation of the primary and secondary of the power transformer, particularly if the power-supply-common is not tied to chassis (AC) ground at the supply. (This is done to avoid resistive coupling of power line currents producing ground system voltage errors.) In multiple power-supply systems, it may be necessary to tie each power common and chassis ground together and accept the resulting ground loops.

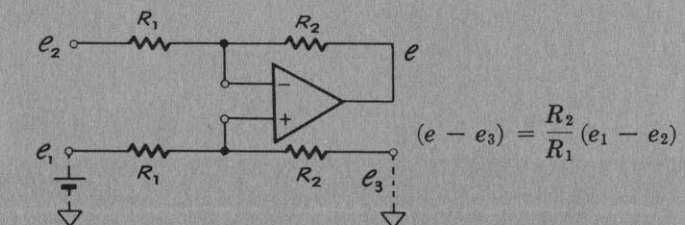
Circuit (c) is a difference amplifier capable of converting a signal referred to one ground system (denoted by  $e_1$ ) to another ( $e_3$ ) in such a way that it makes no difference which (if either) ground system is referenced to the power supplies.

magnetic fields, and a "shorted-turn" effect. Discontinuities in the shield must be avoided; when openings are necessary, minimize dimensions as well as area—i.e., prefer round holes to slits, areas being equal. High-permeability magnetic shielding is *very* well worth its cost, for shielding away signals under 100 Hz, but high-conductivity shielding (aluminum or copper) is the more effective means above 100 Hz. Both resistive and capacitive stray leakage paths, particularly those shunting high circuit impedances, may be interrupted by judiciously-arranged guard rings, as in (c), that lead the coupling to ground or to some other harmless (non-signal) path.

1.30(a)



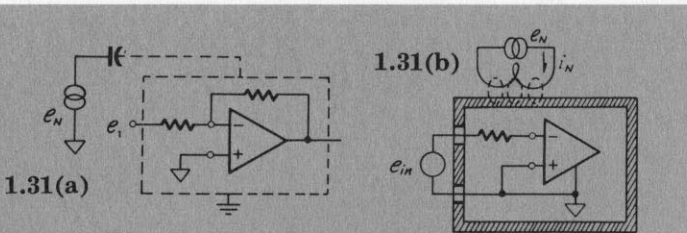
1.30(b)



1.30(c)

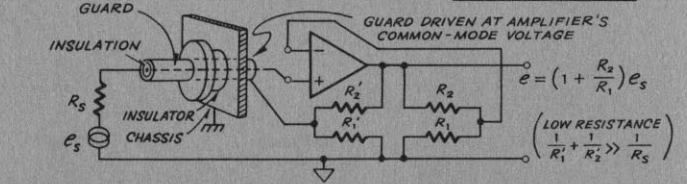
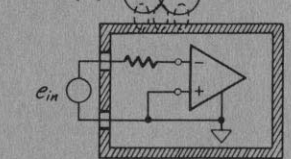
### I.31 SHIELDING AND GUARDING PHILOSOPHY.

The amplifier input is as available to unwanted as it is to legitimate signals. We recommend that you choose one convenient path for signal entry, then make all of the rest inconvenient. When the unwanted signal,  $e_N$ , is capacitively coupled, as in (a), provide a correctly-grounded electrostatic shield for at least the input circuitry, and preferably for the whole amplifier. When the unwanted signal is introduced via inductive coupling, as in (b), such shielding should be ferromagnetic as well as conductive, thus adding electromagnetic isolation, by providing both a low-reluctance short-circuit path for the lines of flux of external



1.31(a)

1.31(b)



1.31(c)

I.30  
I.28  
I.29  
I.31  
I.39

I.31  
I.28  
I.30  
I.34  
I.39



**I.32 DIODES.** Diodes (or transistors connected as diodes) have many applications in analog circuits. Among these are bounding, current selection, voltage selection, and signal steering or gating.

In bounding, diodes are often used in parallel-opposing configurations, so that they never become reverse-biased by more than a fraction of a volt (typically 0.6 V). In these applications, very low leakage and high incremental resistance may be required when the (reverse) voltage drop is of the order of tens of millivolts or less, whereas, in the same application, very low incremental *forward* resistance is valued when the current is high. These can be estimated using the equation for forward current:

$$i = I_0 \left( e^{\frac{qv}{mkT}} - 1 \right) \quad (1-14)$$

where:

$q$  = electron charge

$v$  = voltage drop

$m$  = correction factor, typically between 1 & 2

$k$  = Boltzmann's Constant

$T$  = absolute temperature, degrees Kelvin

$i$  = diode current

The incremental conductance (slope of the current-voltage curve shown)

$$\frac{di}{dv} = \frac{q}{mkT} \left[ i + I_0 \right] \approx \frac{40}{m} \left[ i + I_0 \right] \quad (1-15)$$

**I.33 CAPACITORS.** Capacitors are critical primarily in two kinds of circuits: (1) in Integrators and "Sample-and-Holds," in which a capacitor must be charged precisely, and in which leakage, soakage,\* and (often) exact capacitance value matter most; and (2) in by-passing and sometimes stability compensation ( $C_c$  in I.42a) in which resonance, losses, and sometimes leakage matter most.

Polystyrene capacitors offer the best leakage/soakage combination. For tolerances of the

\*Capacitors with low soakage come up to charge rapidly, without excessive losses, or voltage lag or creep during or after charging.

for bounding and other "switch-function" applications (see I.25 for an example), a low value of  $I_0$  is particularly necessary. The FD300 has proved satisfactory in many applications. It has, typically,  $I_0$  less than  $10^{-11}$  amperes at room temperature, doubling in value with each 8 to  $10^\circ\text{C}$  of temperature rise.

For current selection, switching speed may be an important criterion. A fast diode must have low shunt capacitance (or stored charge) under as much as 0.5 V of reverse bias. For this class of applications, (see II.23) we have used the 1N914 successfully.

When the characteristics of two or more diodes must be matched over a substantial current range, transistors connected as diodes (which have a factor  $m$  of almost exactly 1) are far superior. (See II.22.)

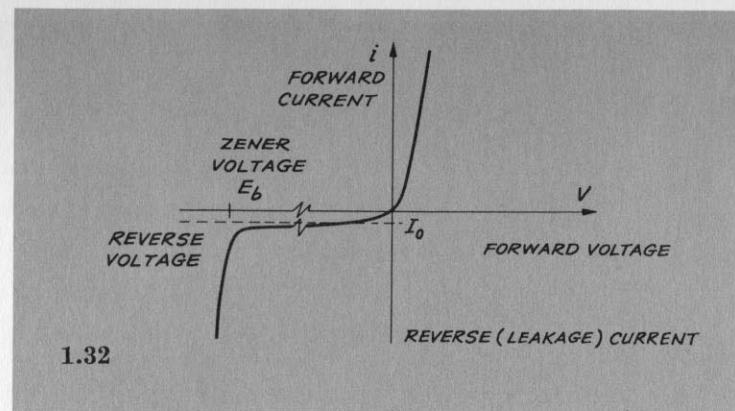
Voltage selection may require that diodes be able to withstand substantial reverse voltage. 1N914 diodes can be used for 10-volt systems, and FD200 diodes work well in 100-volt systems. (See II.34.)

Signal steering or gating applications (see II.36 and II.40) often require diodes with high speed, low leakage, and the ability to withstand significant reverse-voltage. A good choice for a 10-volt system is again, the 1N914.

When very low reverse leakage is required, the collector-base junctions of selected silicon small-

order of 0.01%, we recommend a constant-temperature oven.

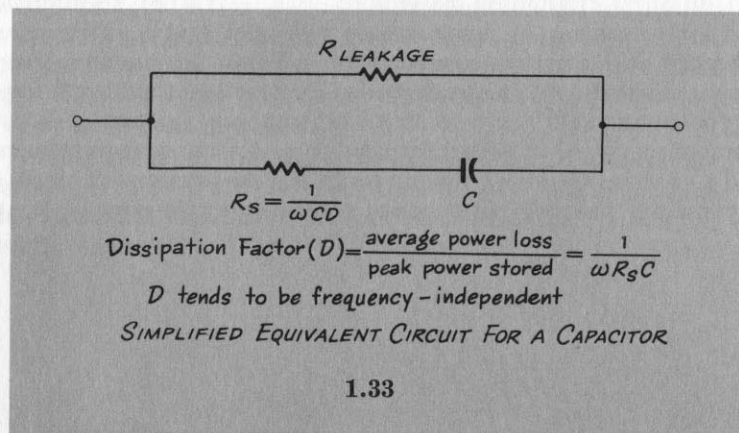
Polycarbonate or mylar capacitors are excellent low-cost alternatives to polystyrene where the ultimate in performance is not required, and they have less leakage than ceramic. In "Track and Hold" circuits for repetitive computation they are quite often entirely adequate—availability is also good. As for leakage in small capacitors, mica capacitors of the MC-15 style dependably exhibit a leakage resistance of at least 7,500 megohms, and the excellent (and unjustifiably maligned) ceramic discs are even better. Our favorite designs typically measure 80–100 thousand megohms.



1.32

signal transistors (such as the 2N930) have been found to be as low in leakage as any commercially-available diodes,\* at reverse voltages as high as 30 volts.

The zener or reverse breakdown characteristic of a diode may be exploited to provide a stable reference voltage. The stiffness of such a reference with respect to loading and to temperature depends upon the current flowing through the diode. Typically two to ten milliamperes of reverse current may be required to achieve optimum temperature insensitivity. For low-voltage applications (less than 10 volts) the base-emitter breakdown characteristic of many transistor types can be used in the place of an expensive and perhaps not readily available zener diode. For this purpose the transistor should be connected as a diode; i.e., base and collector tied together. Breakdown diodes are also commonly used for bounding as recommended in I.25.



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I.32  
I.25  
I.27  
II.22  
II.24  
II.28  
to  
II.31  
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II.35  
III.45  
III.48

I.33  
I.42  
II.10  
II.12  
II.46  
to  
II.48  
III.48  
to  
III.53  
III.56  
III.57

**I.34 CONVENTIONAL RESISTORS.** Resistors are the most important and widest-ranging (in value) of all the external components used in Operational-Amplifier circuits. There are probably more kinds of resistors than there are of any other component. To compound the matter, in some 90% of all our circuits, the ultimate limitation to accuracy and stability is not the amplifier, the power supply, nor any other component, but the *resistors*.

Beyond initial tolerance, the largest component of resistor error is its temperature coefficient. Following closely are: leakage (particularly in values above 100 k $\Omega$ ), humidity effects, drift with time, voltage coefficient, and (rarely in Operational-Amplifier circuits) self-heating and hysteresis after self-heating.

Resistors also exhibit several kinds of noise-generation effects, including thermal EMF's (Seebeck effect), and, as mentioned in earlier sections, stray capacitance across the terminals, as well as series inductance (particularly in wire-wound types), and susceptibility to undesired coupling.

For computing components we use and recommend resistor types in the following order of preference.

**WIRE-WOUND RESISTORS ARE FINE** (1) Nothing beats them for initial accuracy and stability. (2) Their noise levels approach theoretical minima. (3) They are available in many (relatively expensive) special forms: shielded, hermetically sealed, encapsulated, oil-filled, guarded, etc.; small, moderately-priced sealed units in various tolerance ranges are available from several sources. But . . . (4) Above about 1 Megohm, they begin to be quite expensive. (5) Reliable designs much smaller than 1" long x 1/2" O.D. *per megohm* are hard to find. (6) For a given resistance value, they have higher shunt capacitance and series inductance (even the "non-inductive" types) than any other kind of resistor. The smaller they are per megohm, the worse is the reactance problem.

**COMPOSITION RESISTORS** . . . of the familiar military type (Ohmite AB) are excellent choices for experiment and not-so-critical bread board applications but are generally not employed as feedback or feed forward resistors in final operational circuits. These resistors are extremely reliable for almost all other functions in the production of Operational Amplifiers themselves and as low power pull downs, etc.

**THERE ARE SOME GOOD FILM RESISTORS** . . . We like some designs such as the so-called "metal-grid," for (1) their flicker-free behavior and (2) the fact that their "white noise" approaches theoretical. We also like some military grade film resistors because (3) their T.C. range lies within  $\pm 150$  ppm/ $^{\circ}\text{C}$ , (4) their shunt capacitance and series inductance are low, (5) up to 10 megohms, they are highly reliable, and cost less than wirewound resistors.

**FOR VERY HIGH RESISTANCES**, we look to such glass-enclosed, deposited-carbon resistors as are represented by the Pyrofilm and Victoreen designs. The Pyrofilms appear most suitable for the range from 10 megohms to 100 megohms, having (1) very low flicker, (2) T.C.'s in the range of  $\pm 300$  ppm (matched, if we wish, to within  $\pm 5$  ppm), (3) little or no aging effect, (4) excellent reliability. By the way, they are (5) excellent high-frequency resistors—at 10 megohms, only about 0.25 pF! The Victoreen design offers: (6) values to 10,000 megohms, (7) calibration to  $\pm 1\%$  (with compatible stabilities) right up to  $10^{10}$   $\Omega$ , and (8) high reliability, despite the range and accuracy. The glass-enclosure helps tremendously, and it deserves careful consideration as to the insulation on or in which it is mounted, of course.

Speaking of leakage prevention brings us to insulation—one extreme of resistance technology. (The *other* extreme—wiring for low impedance—has come up in I.28 and I.30.) The choice of good insulation for high-resistance circuits, in which leakage must be minimized, might well follow the listing below,\* which has been arranged in the order of decreasing insulation effectiveness, with no regard to many other important properties, such as availability in the desired form, cost, machinability, strength, etc., etc.:

\* Ref: Materials in *Design Engineering* Vol. 62 No. 5 P. 18

Vacuum, Dry gases

Polyethylene, Polystyrene, Teflon (TM)

Mylar

Mica, Glass-filled polystyrene, Polycarbonate (Lexan) (TM)

Polycrystalline glass (treated), Polyvinylchloride, Glass epoxy

Borosilicate glass, Lead silicate glass, Molded epoxy

Cast epoxy, Ceramics (untreated), Silicones

Phenolics (paper based)





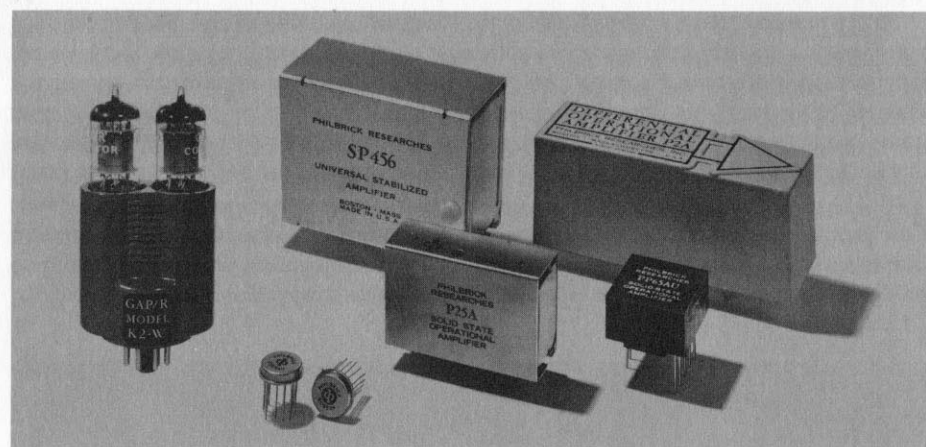
**I.37 AMPLIFIER PERFORMANCE RATINGS.** Throughout this text, the reader will find recommendations as to the performance characteristics of the Operational Amplifiers used in the circuits and applications treated. To assist you in evaluating the suitability of a particular Philbrick Amplifier to a particular application, we have devoted the fold-out back cover to a comprehensive Amplifier Characteristics chart. . . and to speed your use of that chart, we offer this rapid-search table, which rates 18 families of Amplifiers in terms of their salient (●) superior (✓) or outstanding (!) properties. The criteria used are the ones most often mentioned in our circuit descriptions. The recommended procedure is to (1) note the characteristics most desired for the application; (2) use the chart to identify the families likely to satisfy; and (3) examine the detailed characteristics of those families in the Characteristics chart.

**I.37**

	P25A	Q25AH	P35A	P35C	P45A	P45AL	P55A	P65A	P65AH	P75A	P85A	P85C	Q85AH	SP2A	SP65A	SP65AH	SP656	SP456
GAIN			✓	✓	●	●				●	●			!	!	!	!	
BANDWIDTH		✓	●	●	!	●		✓				✓			✓		!	
CMRR	●	●	✓	✓						✓	✓	✓	!					
INPUT IMPEDANCE	!	!	✓	✓				✓	●	✓	✓	✓	!					
OFFSET VOLTAGE	●	●	✓	✓	●	●	●	●	✓	✓	✓	✓		!	!	!	!	
OFFSET CURRENT	✓	✓	●	✓				●	●	●	●		!	!	!	!	!	
NOISE	✓	✓	●	●			●	●		●	●	●	!					
OUTPUT POWER					✓	✓										✓	✓	

**I.37**

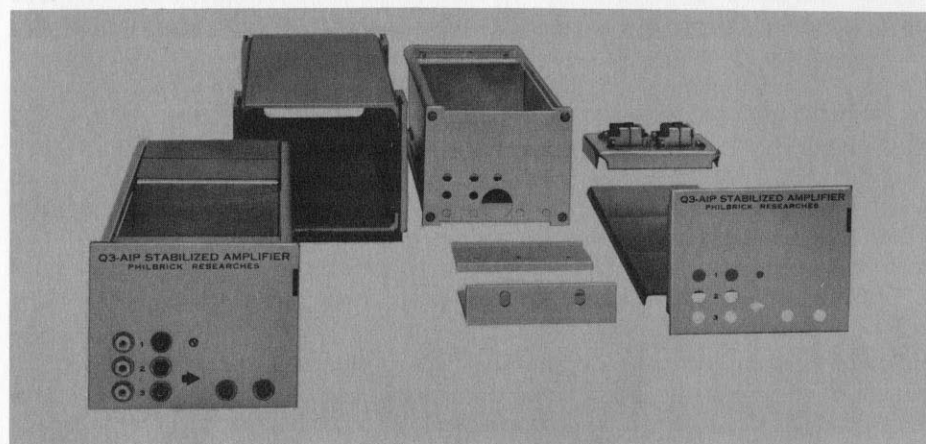
**I.38 STANDARD AMPLIFIER PACKAGES.** An amplifier has no inherent or classic shape of its own, but must be given one—as convenient and unobtrusive a configuration as its components and characteristics allow. Philbrick amplifiers have always been offered in compact and efficient mechanical forms, from the original vacuum-tube models in the electrically and mechanically stable plastic shell, through the newest encapsulated solid-state monoliths. The K2 Series has been augmented by SK2's in all-metal ventilated cases, K2-J militarized versions, and the USA Series of board-mounted units (and militarized counterparts, the USA-J Series). Solid-state condensation has sponsored the metal-cased P Series ( $2\frac{1}{4}'' \times 1\frac{1}{2}'' \times \frac{3}{4}''$ ), and SP Series ( $3\frac{3}{16}'' \times 2\frac{3}{8}'' \times 1\frac{1}{2}''$ ) modules intentionally compatible with the Q3 Modules described in I.39. Their miniature versions, the PP Series and the FP low-profile series are ideal for printed-circuit use. Then there is the cast-aluminum case used for potting such designs as the floating-input P2A. Finally, there is the little newcomer in the TO-8 transistor case, (0.60" diameter, 0.150" high) . . . where will it all end?



**I.38**

**I.39 "HARDWARE" FOR CIRCUIT REALIZATION.** The Q3 Modular Electronic Package shown at right was developed to make the process of translating schematics into equipment quick, economical, and almost painless. Efficiently accommodating a number of Philbrick plug-in units (see p. 96 and cover flap), the Q3 system also offers the equipment designer a broad selection of blank and pre-punched chassis and panels, plug-in circuit boards, and connectors. These extruded-aluminum, 4.2" wide, 3.5" high, 13" long cells can be grouped, stacked, locked together, or assembled into 19" relay rack combinations. Modules slide into their cases from the front, have mating connectors at the rear, and are secured and released by a ball-bearing latch. Thermal, electrostatic, and magnetic shielding are excellent. Q3 is available off-the-shelf.

For the designer with little time for building "from the ground up," there are the Q3-series "Universal Operational Modules," such as Model Q3A1P—self-sufficient devices, in which such distractions as socket-punching, service interconnection, noise pick-up, and instability have been minimized freeing him to concentrate on the signals, and the MP and RP manifolds for multi-amplifier circuitry with less-stringent requirements.



**I.39**  
**I.28**  
**to**  
**I.31**

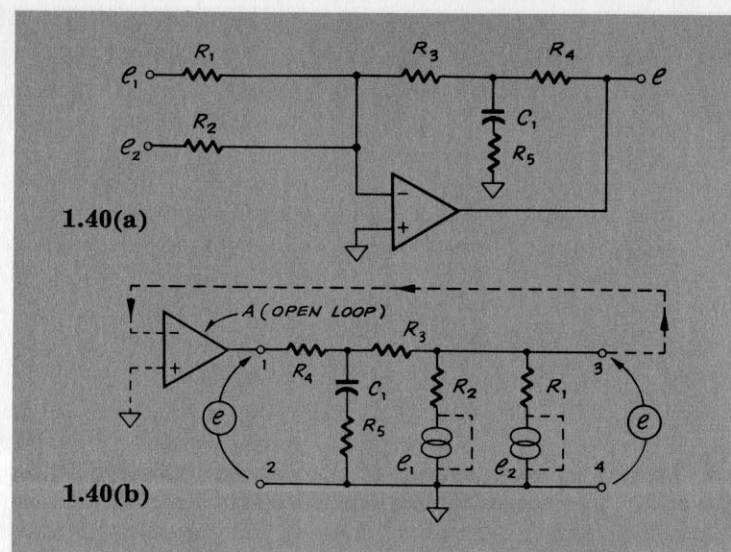


#### I.40 ACTIVATING THE FEEDBACK NETWORK.

It is time that we introduced you to a useful new *attitude* toward Operational Amplifier circuits; one in which the amplifier is treated as an *activator*. This principle in no way alters the functional realities that we have so far discussed—rather, it is intended to *illuminate*, to *organize*, and (with luck) *simplify* those realities. In circuit (a), the feedback network is a trifle messy, but otherwise the elements are all familiar. The *format* of the circuit, however, does not delineate the *activity* about which our equations will be written. Figure (b), on the other hand, does exactly that—it shows the amplifier activating a

complex network made up of all of the impedances in the circuit external to it, and deriving feedback from the network output. Note that we have shown dashed-line shorts across input voltage sources, anticipating the use of Thevenin's Theorem.

To determine the closed-loop gain and stability of a circuit, we shall need to know the transfer characteristic of the network that the amplifier activates. This characteristic is the complex attenuation,  $\beta$ , a function of frequency. Except for the simplest feedback networks, and then only for limited bandwidth, it is often more efficient to use this "activation" approach.



I.40  
I.17  
I.18  
I.26  
I.41  
to  
I.44  
I.51

#### I.41 OPEN-LOOP SET-UP; CLOSING THE LOOP.

It is time to define and examine the relationships amongst the various parameters in the feedback loop. There are five that will concern us, and their small-signal frequency responses may best be characterized by stating their transfer properties, in magnitude and phase. We have already met three of them:

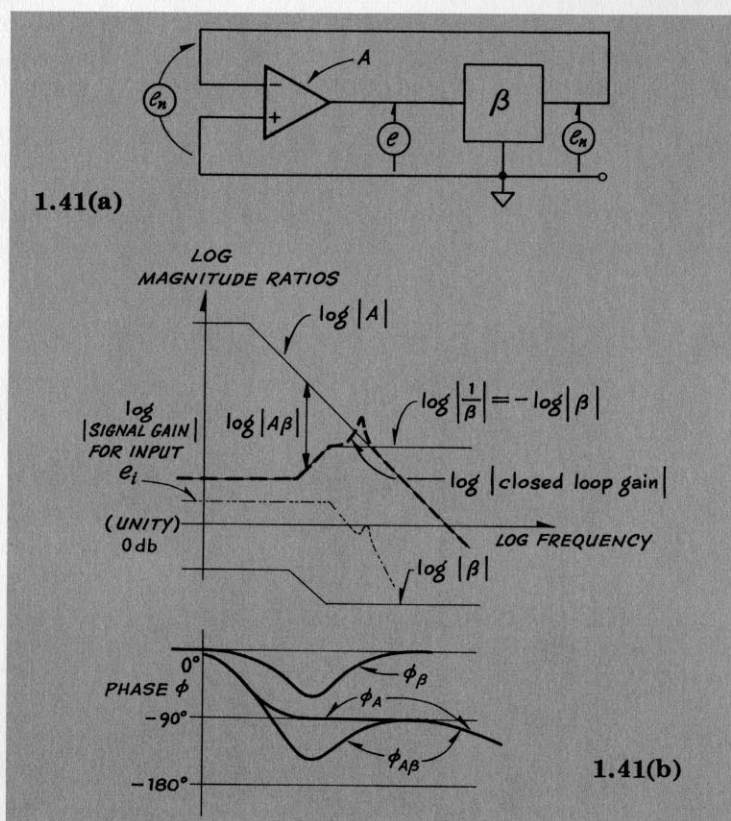
- **Open-loop gain ( $A$ ):** The output/input response of the amplifier itself (i.e., without feedback), all output loads being present; frequency dependent, as discussed in I.17.
- **Feedback-loop attenuation ( $\beta$ ):** The response of the feedback network, accounting for the effects of all impedances in the loop, whether planned, parasitic, or providential. It should be noted that, in the most general case,  $\beta$  may include one or more stages of gain, and Thevenin generator impedances of one or more inputs, as well (I.15). The inverse of  $\beta$ , i.e.,  $1/\beta$ , is often called the "noise gain," because voltage noise is amplified by this factor at frequencies for which the *loop gain* (see below) is large compared to unity.
- **Signal gain:** The response of the amplifier circuit to any one of its input signals. (See, for example, the equation in figure 1.15.)

Let us now consider two additional definitions:

- **Loop gain ( $A\beta$ ):** The net gain as seen when travelling around the loop from any arbitrary point at which the loop has been opened back to itself. The magnitude and phase of the loop gain function is the most meaningful measure of the suitability of a circuit for any planned application, because it tells us the amount of error caused by the fact that the amplifier gain is not infinite, and it also tells us how stable the circuit will be.
- **Closed-loop gain** is the output/input ratio obtained when a voltage signal is inserted in series with either input of the amplifier. Closed-loop gain is, incidentally, the *true noise gain*. It is defined as follows:

$$\text{Closed-loop gain} \equiv \frac{1}{\beta} \cdot \frac{1}{1 + \frac{1}{A\beta}} \quad (1-16)$$

The curves in (b) depict a consistent set of gain and phase relationships amongst the above parameters for a hypothetical (but conventional) amplifier and feedback circuit.



I.41  
I.17  
I.18  
I.26  
I.42  
to  
I.44  
I.51

**I.42 ACHIEVING DYNAMIC STABILITY.\*** Operational Amplifier techniques always employ feedback. Not all feedback circuits produce stable conditions; some are definitely *unstable*, and oscillate more or less freely, while others are only *conditionally* stable, and lie in wait for a signal (or other) condition that will stimulate them to oscillate . . . either form of instability will render the circuit useless, unless it is to be a signal source of some kind (with controlled instability), of course.

Fortunately, there are only two sources of instability: conceptual oversights in planning the feedback network, and “stray,” or otherwise unsuspected, circuit elements that significantly modify the feedback circuit—from the sane and stable form originally planned, to the “bomb” one observes under test. Remember this: *There Is Always A Way Out*, however elusive it may seem at first.

Predicting the dynamic stability of the closed feedback loop around an operational amplifier is accomplished in the same way as it is for any servo or feedback system. A useful analytical attack is to diagram the loop in a way that makes it easy to visualize—one such way being shown in (b).

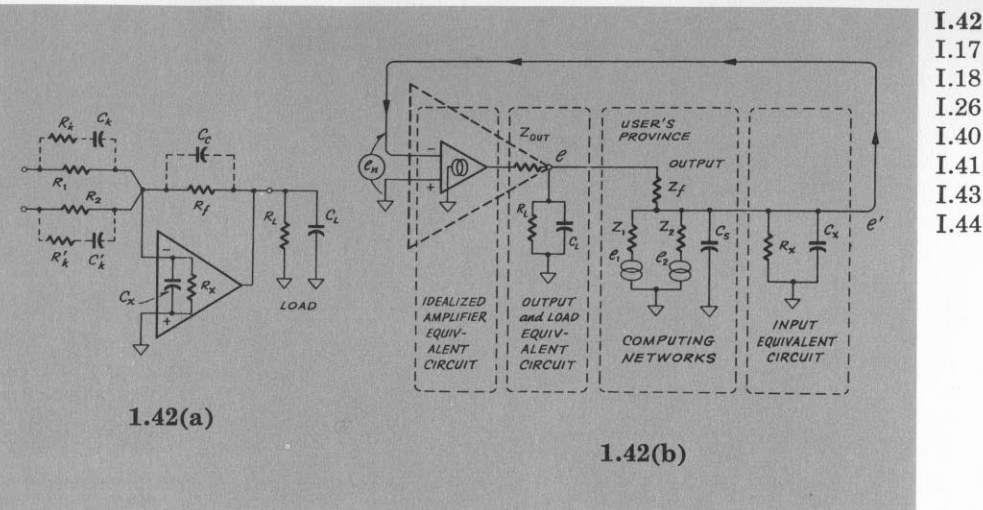
In this attack, the actual amplifier is represented as an idealized operational amplifier that is preceded and followed by equivalent circuits describing its departure from the ideal. (Glance back to I.7.) These two equivalent circuits surround the computing-feedback network; all three are interdependent. Together, they may be reduced to a single network, through which the loop around the ideal amplifier is closed. It is helpful to arrange the “composite” network in such a way as to emphasize the effect of the *external* part of the network—the part under *your* control—on the overall phase-attenuation characteristics.

Small-signal frequency response of a typical Operational Amplifier may be expressed algebraically by:

$$\text{gain} = - \frac{A_0}{1 + jA_0 \frac{\omega}{\omega_H}} \cong +j \frac{\omega}{\omega_H}$$

where:  $\omega$  = any angular frequency in radians/sec, and  $A_0$  = the value of the “DC” or low-frequency gain.

We have also shown (and the mathematics implies) that the phase shift of such an amplifier is a constant  $90^\circ$ , so long as the roll-off is uniform at 20 db/decade. Unfortunately—see Figure 1.17 (b)—the amplifier phase lag may increase rapidly at frequencies near and above  $\omega_H$ ; so that the stable, useful negative feedback we require can become *positive* feedback, at some frequency. If the frequency at which that occurs is above  $\omega_H$ , then the gain will be below unity, and sustained oscillation by the amplifier alone, even fully fed back, is not possible. Unfortunately, it is not merely the amplifier that can cause phase lag; circuit (b) shows that. Even ignoring the effect of load capacitance (which may well be negligible in many applications, compared to  $Z_0$ ) we must acknowledge that  $C_x$ , the input capacitance, in combination with  $Z_f$ , can, and usually does, cause significant phase shift at frequencies lower than  $\omega_H$ . We have already mentioned a simple



solution to this problem, in I.18, and that solution is shown in dashed lines in Figure (a)—a small capacitor,  $C_c$ , so proportioned that:

$$C_c R_f = R_{in} C_s \quad (1-18)$$

where  $R_{in}$  is the composite Thevenin impedance obtained by paralleling  $R_1$ ,  $R_2$ , and  $R_x$ . In practice, a larger value of  $C_c$  is often used if small bandwidth (for slow response or low noise) are desired. However, equation (1-18) is usually very conservative, and if maximum bandwidth is desired, a value of  $C_c$  much smaller than the one it advocates can often be used, providing very fast response, yet still ensuring good dynamic stability. In practice, this value is usually determined empirically, by trimming  $C_c$  down until the desired response is obtained. Another way to compensate for the lagging effect of  $C_c$  is to add another compensating network, also shown in dashed lines in I.42(a), and labelled  $R_k$ ,  $C_k$ , and  $R'_k$ ,  $C'_k$ , proportioned so that:

$$R_1 C_k = R_2 C'_k = R_f C_c \quad (1-19)$$

with

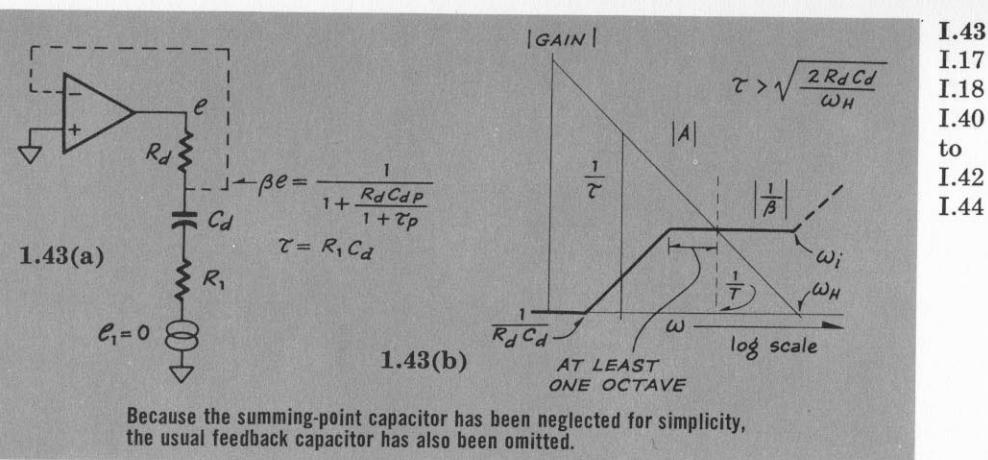
$$R_k \cong \frac{1}{100} R_1, \quad R'_k \cong \frac{1}{100} R_2$$

Another source of dynamic instability may be the presence of capacitive load,  $C_L$ . In most modern solid state amplifiers, a  $C_L$  of up to a few thousand picofarads is not harmful, so long as some reasonable value of  $C_c$  is used. When a heavier capacitive load than that must be driven, the techniques described in I.44 may be required, to maintain dynamic stability.

\* See also Philbrick Applications Brief R1: *Practical Closed-Loop Stabilization of Solid State Amplifiers*.



**1.43 SAMPLE STABILITY CALCULATION.** The Bode plots for differentiator (a) are shown in (b). Assume that they intersect at the radian frequency  $1/T$  with a net variation of minus 20 db per decade. Then, determine the net sum of all first-order break frequencies to the left of the intersection (leads positive, lags negative in the function  $A\beta$ ).  $1/T$  must be at least twice the sum, which is labelled  $1/\tau$ . Then determine the net sum of all time constants to the right of the intersection (lags positive, leads negative in the function  $A\beta$ ).  $\tau$  must be at least twice this sum, which is labelled  $1/\omega_i$ . If one but not both of the above-stated conditions is satisfied as an equality, the closed-loop system will have well-damped roots, since the open-loop characteristic ( $A\beta$ ) will have a phase margin of  $60^\circ$  at unity. This simple technique leads to a closed-loop input-output characteristic that approaches ideal behavior at frequencies substantially less than  $\omega_n = 1/T$ , is down about 3 db at  $\omega_n$ , and is lagged above  $\omega_n$ . The transient response has perhaps 5% overshoot and a mean delay time of  $T$  if the ideal characteristic is a constant gain. The differentiator shown departs from the ideal at  $\omega_c = 1/\tau$  (see II.21).

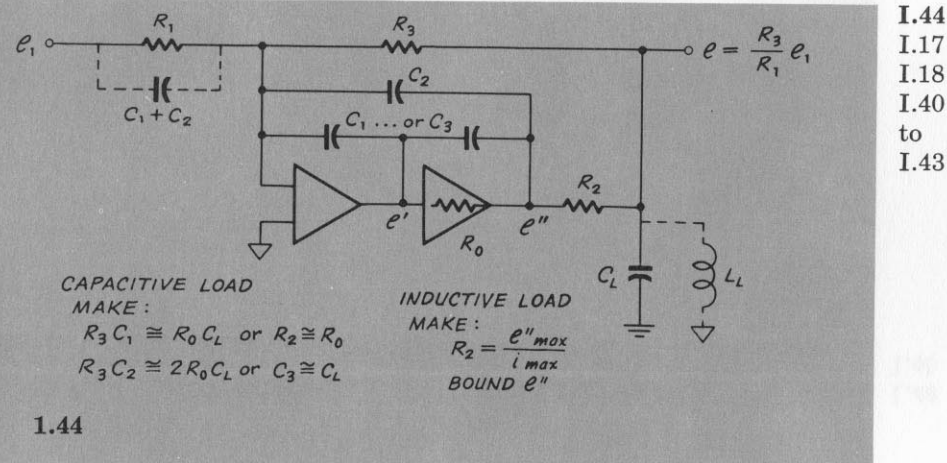


**1.44 AMPLIFIER STABILIZATION WITH REACTIVE LOAD.** A capacitive load may, if  $C_L$  is high, prove difficult to drive. For rapid rates of change of output voltage, large load currents may be demanded, since

$$i_L = C_L \frac{de}{dt} \quad (1-20)$$

and a booster may be needed. The effect of capacitive load on most unboosted Philbrick solid state amplifiers (2 mA output rating) is an effective reduction of the open-loop gain-bandwidth product due to current limiting. On the other hand, a booster decouples its input from the load in such a way that a capacitive load introduces an additional lag,  $R_0 C_L$  (where  $R_0$  = booster output resistance), into the composite amplifier-load characteristic. The closed loop may tend toward instability, particularly if the noise gain,  $1/\beta$ , is near unity at a high frequency as with a follower, inverter, or bounded amplifier. Our usual crutch, the feedback capacitance, will not help and may even make the situation much worse by increasing the net lag.

Instead, at high frequencies the load must be isolated from the point from which the feedback signal is derived, or the booster must be effectively by-passed for high frequencies. In the figure, the booster may serve to isolate the load so that the small high frequency feedback capacitor,  $C_1$ , may be effective. The load may also be isolated by the resistor  $R_2$  (chosen to be about the size of  $R_0$ , perhaps 50) so that the small capacitor  $C_2$  will successfully stabilize the circuit. Note that the output voltage range will be less than that of  $e''$  or  $e'$  when large load currents flow. The booster may be by-passed with a large capacitor,  $C_3$ , chosen



to be about equal to the load capacitance, such that the unboosted output,  $e'$ , drives the load at high frequencies and during sudden transients, the booster being effective for comparatively slowly-varying signals only. In a particular case, one or more of these measures ( $C_1$ ,  $R_2$  &  $C_2$ , or  $C_3$ ) may prove most helpful in taming a heavily-capacitive load.

A shunt inductive load presents a problem at low frequencies, where its reactance is very low. The load current must then be limited by a resistor such as  $R_2$  in the figure. A bound circuit from  $e''$  to the summing point would enable the amplifier to recover immediately after an overload.

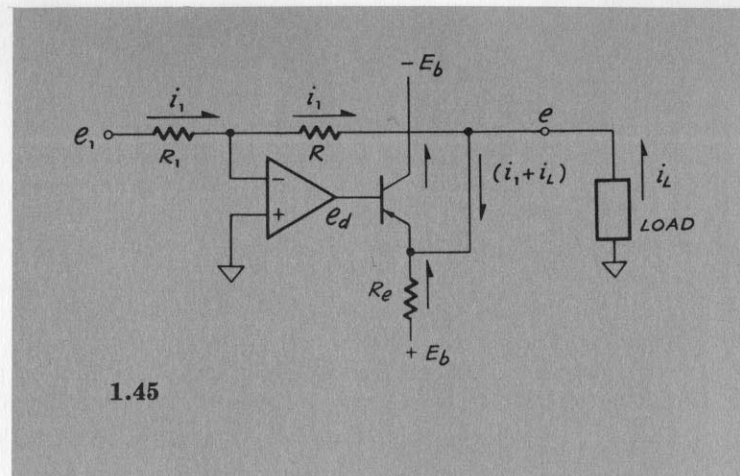
### I.45 EMITTER-FOLLOWER BOOSTERS.

When necessary to deliver more current than may be obtained from a general-purpose Operational Amplifier (designed primarily for high voltage gain and economy of power consumption), the designer can often use standard types having more power output. Often, however, he must find some way to "boost" the current capabilities of any amplifier without visibly deteriorating any of its other characteristics, notably its closed-loop voltage gain and frequency response (if the booster contributes no phase shift below  $f_H$ ). The simplest arrangement is an emitter-follower (or a cathode follower, for vacuum-tube circuits) as a simple unity-voltage-gain device having sig-

nificant current gain and more current capability. Furthermore, the impedance transformation (and subsequent unloading) provided can *greatly increase* the open-loop gain of the main amplifier.

The single-transistor emitter-follower is most efficient when used to supply output currents of only one polarity. For positive output currents, use an NPN type; for negative output currents use a PNP. For both high efficiency and impartial performance, see I.46 below.

A resistor should be connected in series with the collector to protect the transistor against excessive short-circuit current. Bypassing that resistor with a capacitor will allow unimpaired high-frequency response.



1.45

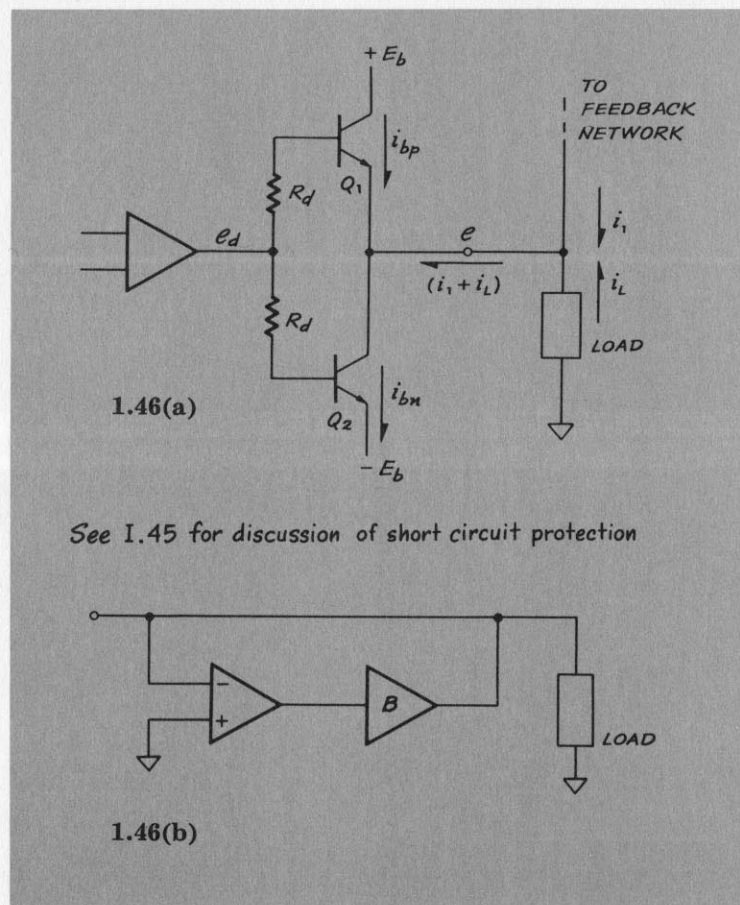
I.45  
I.46

### I.46 HIGH-EFFICIENCY BOOSTERS.

Circuit (a) constitutes a significant improvement over the emitter-follower circuit of the preceding section. It uses a complementary pair of transistors, the idling current of which can be made negligible, without in any way limiting the output current capability of the booster. For positive-going drive signals ( $+e_d$ ),  $Q_1$  delivers the required output current, while  $Q_2$  loafs essentially at cutoff. For negative going drive signals ( $-e_d$ ),  $Q_2$  does all the work, while  $Q_1$  lolls at or near cutoff. The dynamic voltage range of this circuit is far wider than that of the emitter-follower for the same power supply and drive parameters, yet its efficiency is many times higher; in fact, if the maximum output voltage range required is lower than the nominal power supply voltages used for the amplifier,  $+E_b$  and  $-E_b$  may be made quite small (perhaps a volt or so more than the required peak swings), further increasing the efficiency of this superior circuit.

Circuit (a) does not satisfy by any means all of the requirements imposed upon a practical booster for general-purpose use. Current-limiting problems, not entirely solved by  $R_d$ , are only one subset of several such practical problems. Moreover, the design of efficient voltage (or voltage-cum-current) boosters presents a far-from-trivial challenge. Such boosters, if realized, would make it practical for conspicuously non-muscular amplifier, such as Philbrick P65Q... operating "starved," at that, to control a watt at  $\pm 100$  volts.

Fortunately, however, there is a simple—and a thoroughly satisfactory—solution to the whole booster problem: Philbrick Booster Amplifiers, which are available in packages compatible with all major amplifier lines, and in designs compatible with standard Philbrick amplifier power supply voltages. These are described in the Philbrick literature and are enticingly portrayed as shown in Figure (b): simply by a triangle marked "B."



1.46(a)

1.46(b)

I.46  
I.45

See I.45 for discussion of short circuit protection

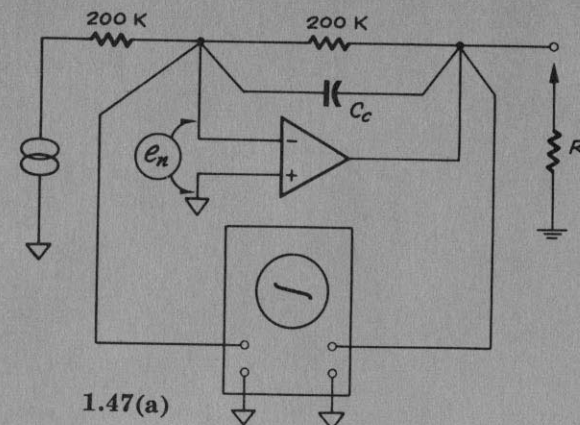


**I.47 MEASURING OPEN-LOOP GAIN.** In this and the four modules that follow, we shall be discussing means of measuring the performance of an Operational Amplifier—not necessarily *in situ*, but sometimes in special test circuits designed to render such tests practical and accurate, and hence easy and meaningful. Such a special test circuit, designed to measure the open-loop gain and phase characteristics of an amplifier over a range of frequencies, is shown to the right in figure (a). It will be recognized as a simple unity-gain inverter, with the stabilizing capacitor,  $C_c$ , that we have now learned to add almost automatically to such circuits. Having established the standardized operating conditions—power supply voltage, temperature, etc., we are now prepared to feed a signal into the inverter and examine the Lissajous pattern produced by feeding the summing-point signal into the vertical channel of an oscilloscope and feeding the output voltage into the horizontal channel. An external load resistor may be connected or not, as desired.

We can write the expression for the gain of the amplifier as:

$$\text{gain} = A = \left| \frac{e}{e_n} \right| \quad (1-24)$$

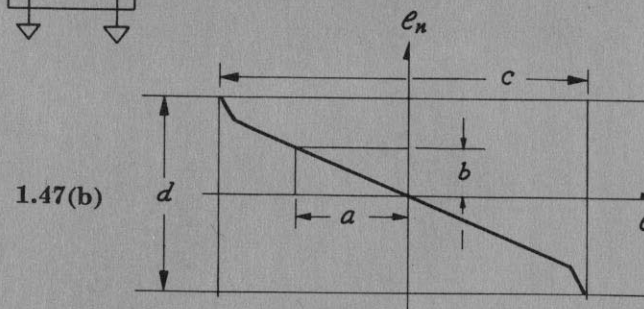
so that either the incremental or the peak gain can be read from the oscilloscope as shown in figure (b). If amplifier gain is exceptionally high, or if an oscilloscope with adequate vertical sensitivity is not available, the amplifier can be used to “preamplify its own voltage error,” as shown in (c), in which the vertical sensitivity of the oscilloscope is made effectively 101 times as great as its nominal value. Since this high gain applies to dc signals as well as ac, the voltage offset adjustment should be made carefully, to avoid saturation of the CRO. So long as the input impedance of the amplifier is much higher than 1 k $\Omega$ , this technique is valid; at high frequencies, however, circuit (c) is neither necessary nor recommended, and circuit (a) should be used. As frequency is increased beyond very low frequencies, the oscilloscope display will gradually become elliptical because of amplifier phase shift (see I.41). The AC voltage gain magnitude and phase for any particular frequency can be read from the oscilloscope as shown in figure (d). At very high frequencies, rate limiting will show up as distortion (see I.17) and the output-signal test amplitude must be reduced in order to make meaningful measurements of small-signal (linear) response. The input capacitances of the oscilloscope, and the feedback capacitance,  $C_c$ , will not affect the accuracy of the measurements, but the high frequency amplitude response and the relative phase shifts of the oscilloscope amplifiers over the entire frequency range should be verified as acceptable.



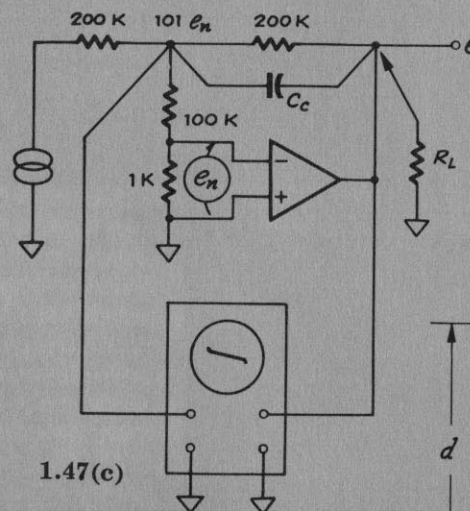
1.47(a)

$$\text{INCREMENTAL } A = \frac{a}{b}$$

$$\text{PEAK-TO-PEAK } A = \frac{c}{d}$$



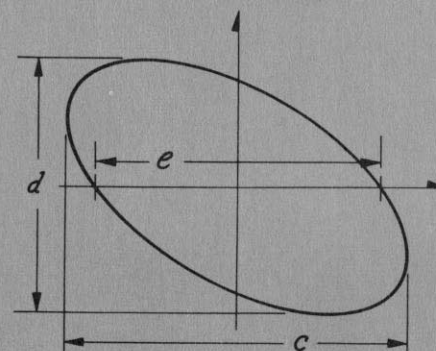
1.47(b)



1.47(c)

$$\text{AC VOLTAGE GAIN} = \frac{c}{d}$$

$$\text{PHASE LAG } \phi = -\sin^{-1}\left(\frac{e}{c}\right)$$



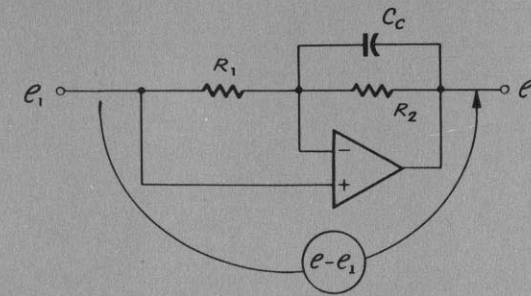
1.47(d)

**I.48 MEASURING COMMON-MODE REJECTION.** In this circuit it is best to make the ratio  $R_2/R_1$  some simple integral value, about one tenth to one hundredth of the  $CMRR$  one expects to find, using moderately low resistances to set up the ratio. The value  $(e - e_1)$  is best measured on an instrument with a true differential input, such as a differential DVM, a floating CRO, or a VOM. The  $CMRR$  is defined as inversely proportional to the magnitude of  $(e - e_1)$ , for a fixed common-mode swing. This circuit is especially well

suited to amplifiers having very high no-load voltage gain . . . much higher than the expected  $CMRR$ . (See I.47 for measurement of  $A$ .)

$$(e - e_1) = \left( \frac{R_2}{R_1} + 1 \right) \left( \frac{e_1}{CMRR} + \frac{e}{A} \right) \quad (1-25)$$

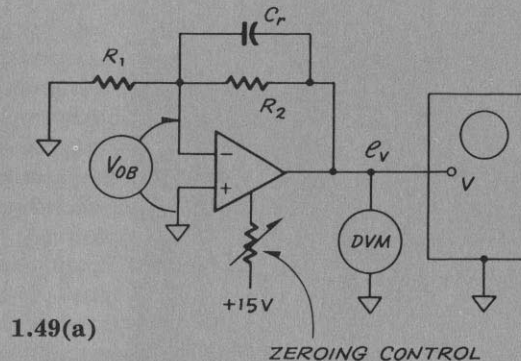
$$CMRR \cong \left( \frac{e_1}{e - e_1} \right) \left( \frac{R_2}{R_1} + 1 \right) \quad (1-26)$$



1.48

**I.49 MEASURING "DC" OFFSETS.** Circuit (a) may be used to determine the voltage offset of an amplifier. For good sensitivity it is preferable to make  $R_2$  at least 100 times as high as  $R_1$  so that the oscilloscope or digital voltmeter used to read the output will be able to operate on a convenient range. On the other hand, the greater the circuit-gain, the lower the loop-gain, which may introduce a (definitely second order) finite gain error factor.  $C_r$  is used to limit the bandwidth to low frequencies, so as to prevent the masking of voltage offset by noise. The procedure is simple: obtain the best zero adjustment possible, if one is present, and read the output voltage. The equation shown may then be solved to relate  $e_v$  to  $V_{OB}$ .  $R_1$  and  $R_2$  should be kept at the lowest feasible values, to prevent current offset from superimposing its effect on the voltage offset measurements. 100  $\Omega$  and 10 k $\Omega$  or 100 k $\Omega$  are suitable values, for example.

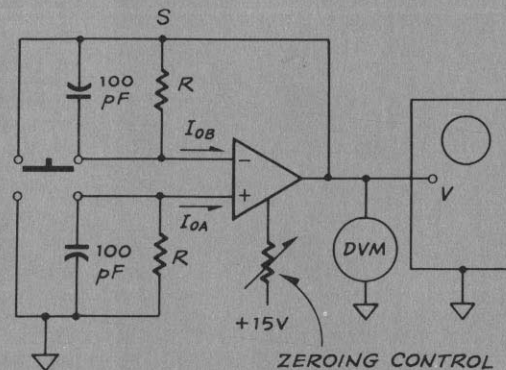
Circuit (b) provides a means of measuring the input current to each terminal, independently. If the voltage offset measurement has just been made, the zeroing control should be left in that position, unless it is intended that the voltage offset be adjusted to compensate for current offset. Output measurements are then made for both positions of the switch, and the two results translated into equivalent currents, as shown on the diagram. Note that it is possible to obtain increased sensitivity for this measurement, if necessary, when low currents are being measured by attenuating the feedback to points in the same manner as was done in (a). Note also that if the switch can simultaneously close both circuits, the amplifier's voltage offset can be zeroed. If both circuits are simultaneously opened, the difference of the input currents can be measured.



1.49(a)

#### VOLTAGE OFFSET

$$V_{OB} = \frac{e_v}{1 + \frac{R_2}{R_1}}$$



1.49(b)

#### INPUT CURRENT

$$I_{OB} = \frac{e_v}{R}$$

$$-I_{OA} = \frac{e_v}{R}$$

$$10^6 < R < 10^8$$

MEASURE	SWITCH
$I_{OA}$	UP
$I_{OB}$	DOWN

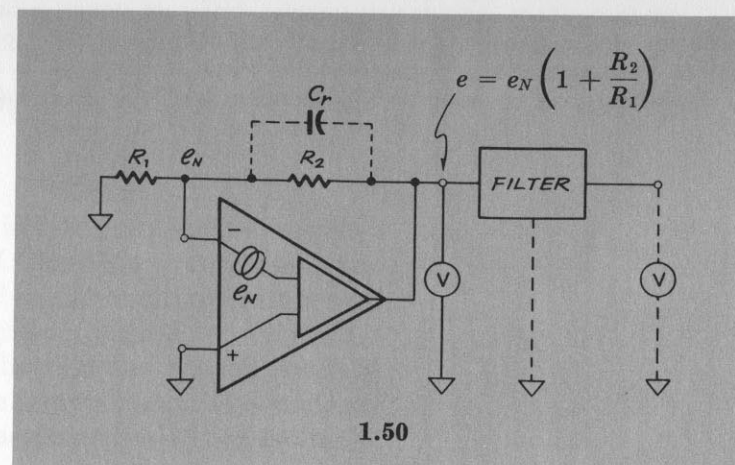
I.48  
I.16

I.49  
I.7  
I.8  
I.11  
I.12  
I.14  
I.15  
I.18  
to  
I.23



**I.50 MEASURING VOLTAGE NOISE AND FLICKER.** This circuit may be used to measure the noise and flicker of an amplifier, provided that the following conditions are imposed upon its use: (1) That  $R_1$  be sufficiently low so that current noise components of the amplifier and thermal noise generated in it may be neglected; (2) That some means (like  $C_r$ ) be employed to limit the measurement bandwidth to that over which the amplifier will ultimately be used... or to that for which the noise rating that is being checked is specified; (3) That the measuring instrument ( $V$ ) whatever it be—from an RMS voltmeter to a peak-to-peak device, such as a CRO—have adequate (but not too great) bandwidth to perform the

measurement, and; (4) That every possible precaution be taken to insure good grounding and shielding, and minimum stray coupling of any kind. If several noise bandwidths are to be examined, or if it is desired to limit the noise bandwidth in a more exact fashion than by the gradual roll-off effect of  $C_r$ , it is probably better to interpose the filter shown on the drawing between the output of the amplifier and the measured instrument. This filter may be of the adjustable low-pass/band-pass/high-pass design commonly used in noise and vibration analysis (and it can of course be an active one assembled with operational amplifiers.) (See III.22–28.)

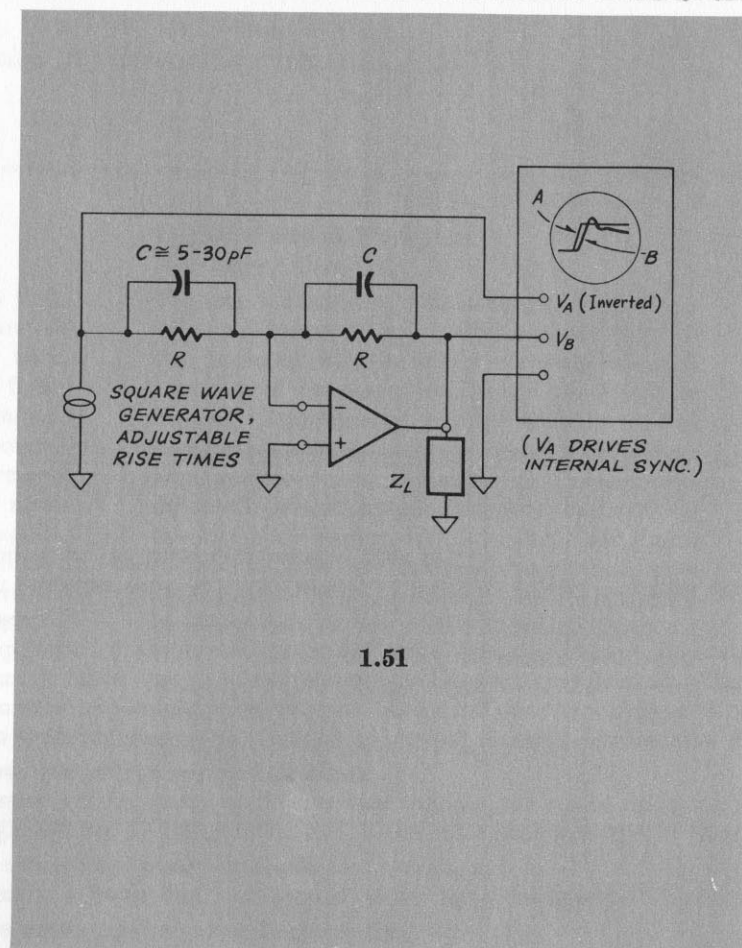


I.50  
I.7  
I.9  
I.10  
II.22  
to  
II.28

**I.51 MEASURING TRANSIENT RESPONSE.** There is no single circuit that will test the transient response of an amplifier under all possible ultimate-use conditions. (It may well be possible to set up the ultimate-use circuit, however, and run a test of the type we are about to describe, and this possibility should not be over-looked.) The circuit shown here will, however, provide enough information to permit a meaningful prediction of the transient behavior of the amplifier in most circuit configurations. The amplifier is connected as an inverter, and is driven from a pulse or square wave generator having adjustable rise and fall times, and a good, distortion-free output attenuator.  $R$  is set to a value comparable to the net input circuit resistance that is anticipated, and the amplifier is loaded with an impedance as close to the ultimate-use circuit as possible. A dual-channel CRO having much greater bandwidth than the amplifier under test is used to monitor both the input and the output signals.

high frequency break-point in the gain characteristics is simple and easily calculated. Unfortunately, there *are* both propagation and magnitude non-linearities in any Operational Amplifier, so that the large-signal response characteristics may bear very little relationship to those predicted by the small-signal curves. In particular, the inability of the circuit to “slew” at a rate demanded by large-signal, fast output transients causes what is known as “rate-limiting.”

The test procedure is as follows: (1) Starting with the smallest signal that may be conveniently viewed on the  $V_B$  channel of the CRO, superimpose the starting points of both  $V_B$  and  $V_A$  (with  $V_A$  “inverted” by the CRO controls) and determine the fastest rise time at which they may be made to coincide within reasonable limits. This rise time is a measure of the small signal transient response; (2) Increase the amplitude of the input, decreasing the sensitivity of both channels of the CRO proportionately, until rate limiting is evident. A further increase in amplitude should cause even further divergence; (3) If the maximum output amplitude is known, one may set it up on  $V_A$  and then increase the rise time until  $V_A$  and  $V_B$  appear to be identical. That rise time is a measure of the maximum slewing rate of the amplifier for that amplitude of output signal.



I.51  
I.17  
I.18  
I.40  
to  
I.44

Let us refresh our understanding of the open-loop gain-versus-frequency characteristics of the amplifier by referring back to I.17. If non-linearities do not exist, the transient response of an amplifier may be predicted exactly from the gain and phase characteristics. The relationship between the fastest rise time that the amplifier will pass without distortion and the

**I.52 NOISE CALCULATIONS . . . NOISE GAIN . . . MINIMIZING NOISE.** For an example of how to make a noise calculation, we shall use the circuit of Figure 1.6. The response to a noise current,  $i_s$ , injected at the negative summing point, and to a noise voltage,  $e_s$ , in series with one of the inputs (assuming an otherwise ideal amplifier) is:

$$|e|^2 = \left| \frac{Z}{Z_0} + \frac{Z}{Z_1} + 1 \right|^2 |e_s|^2 + |Z|^2 \left[ i_{NB}^2 + 4KTB \Re \left( \frac{1}{Z_0} + \frac{1}{Z_1} + \frac{1}{Z} \right) \right]$$

$$e_{RMS} = \left| \frac{Z}{Z_0} + \frac{Z}{Z_1} + 1 \right| (e_s)_{RMS} \sqrt{1 + \frac{\frac{1}{R_s}}{\frac{1}{Z_0} + \frac{1}{Z_1} + \frac{1}{Z}}}$$

Note that  $\left( \frac{Z}{Z_0} + \frac{Z}{Z_1} + 1 \right) = \frac{1}{\beta}$ , which is called the *noise gain*, and  $R_s = \frac{e_{sRMS}}{i_{sRMS}}$  is called the *characteristic noise resistance*.

To minimize the noise-to-signal ratio at the output:

- Use as small a noise gain (as high a value of  $\beta$ ) as possible, without reducing signal gain below an acceptable minimum.
- Design the circuit to function at the lowest practical impedance level. This reduces the influence of  $i_s$ , and also reduces the effect of thermal noise generated by the network resistors.
- Minimize external sources of  $e_s$  and  $i_s$ , by taking sensible precautions to prevent excessive pickup. This includes providing adequate shielding of the summing point—from power lines, chopper-drive excitation, signal lines, and from r.f. radiation. Summing-point leads should be as short as possible.
- Select an amplifier with suitably low (internally-generated) voltage and current noise, in the frequency band of interest.

● To the reader: this page will undoubtedly be filled with a *miscellany of afterthoughts* in forthcoming editions. Meanwhile, the remaining  $\frac{2}{3}$  of this page,  $\frac{1}{3}$  of page 62, and *all* of pages 103 and 104, as well as the margins and other blank spaces, are available for notes, calculations, circuits, inventions, etc.



## PART TWO COMPUTING CIRCUITS

The earliest applications of operational amplifiers were in computational structures applied to indirect modelling, called *analog computers*. In this Part, we present circuits that have found, or are likely to find, their principal employment by members of the computing trade, regardless of their persuasion—*analog*, *digital*, or “*hybrid*.” These circuits will readily be seen to have applications beyond the limited scope of problem-solving and data-handling, and a number of the more articulately-rendered circuits in the “*instrument*” section will be recognized as directly derived from the simple, basic configurations described here.

For convenience, for order, and for other good reasons, this Part has been divided into three sub-plots: *Linear Circuits*; *Continuous-Function Nonlinear Circuits*; and *Discontinuous-Function Nonlinear Circuits*.

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### Linear Circuits

Though these circuits are inherently linear (i.e., output magnitudes bear a directly proportional relationship to input magnitudes), bear in mind that they are often used successfully in combination with *nonlinear* devices and circuitry; either in the same Amplifier circuit, or in league with other Operational Amplifiers. Naturally, no claim to comprehensiveness is made here, either in diversity or in detail, but enough circuits are provided to encourage the Thoughtful Reader to expand on the basic ideas here discovered, and, so armed and stimulated, to crash through to solutions of his specific (and perhaps unique) problems.

**Modules II.1-II.21 . . . pages 39–49**

### Continuous-Function Nonlinear Circuits

If linear circuits are best characterized by their fundamentality and ubiquity, the circuits in this second subdivision are most notable for their *permutability*—the range and diversity of function that may be achieved by combining, superimposing, or reiterating them. Small wonder that we can here give only a representative and—we hope—intelligent sampling of the most powerfully potent of the genre! Once again, many of the seeds planted here will be found flowering in Part III, in the form of Instruments of bold ambition and gratifying competence.

**Modules II.22-II.33 . . . pages 50–55**

### Discontinuous-Function Nonlinear Circuits

Veteran followers of Philbrick publications (a calloused lot) will find nothing remarkable in the generous way in which we embrace such elements of the ungainly Digital Discipline as flipping, flopping, and gating. Indeed, we feel no such reluctance—most of these circuits were born *analog*—and find themselves in their constricted hysteretical, or schizophrenic condition because they have been driven to their limits . . . accidentally at first, perhaps, but now deliberately. Mad and misshapen though they be, they can be very useful indeed, and we value the end above the means, if the blood lines are right. (Digits are members of the Analog family.)

**Modules II.34-II.51 . . . pages 56–62**

**II.1 UNITY-GAIN INVERTER.** A voltage inverter, or one-to-one electronic lever, is formed by using identical impedances in the input and feedback paths. The impedances are usually purely resistive, but sometimes the use of identical reactive or complex impedance elements will improve the overall frequency response.

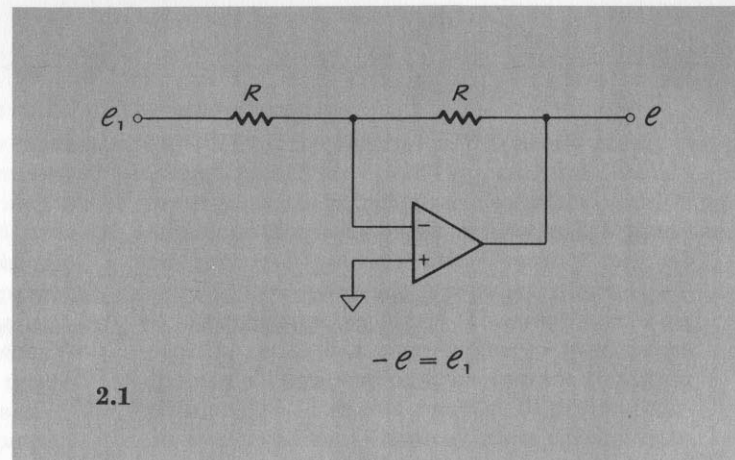
The equation for the inverter response (ideal) may be derived from the general equation (1-4) for this configuration, introduced in I.6, by substituting  $Z$  for both  $Z_1$  and  $Z_2$ , thus:

$$e = -\frac{Z_2}{Z_1} e_1 = -\frac{Z}{Z} e_1 = -e_1 \quad (2-1)$$

Inverters are used wherever sign changes are necessary, or simply to lower the impedance level (and raise the power level) of a signal. In the circuit shown, the output impedance is usually less than an ohm, whereas the input impedance is:

$$Z_{in} = \frac{e_1}{i_{in}} = R \quad (2-2)$$

This circuit functions well over a very wide range of impedances, signal levels, and frequencies. Noise, DC offset, and drift determine the minimum practical signal; and amplifier input current, Johnson noise, leakage, bandwidth requirements, and (possibly) pickup limit the maximum value of  $R$ .



2.1

II.1  
I.5  
to  
I.7  
II.3  
II.6  
II.9

**II.2 THE FOLLOWER.** The follower circuit of (a) has essentially unity gain because the output,  $e$ , is fed directly back to the negative input as degenerative feedback at high gain. It has very nearly unity gain over a wide frequency range, provided that the amplifier has excellent differential properties and high gain.

The follower is ideal for isolating and driving other circuits, as well as for direct signal detection at low energy... and it preserves the sign of the signal (is non-inverting).

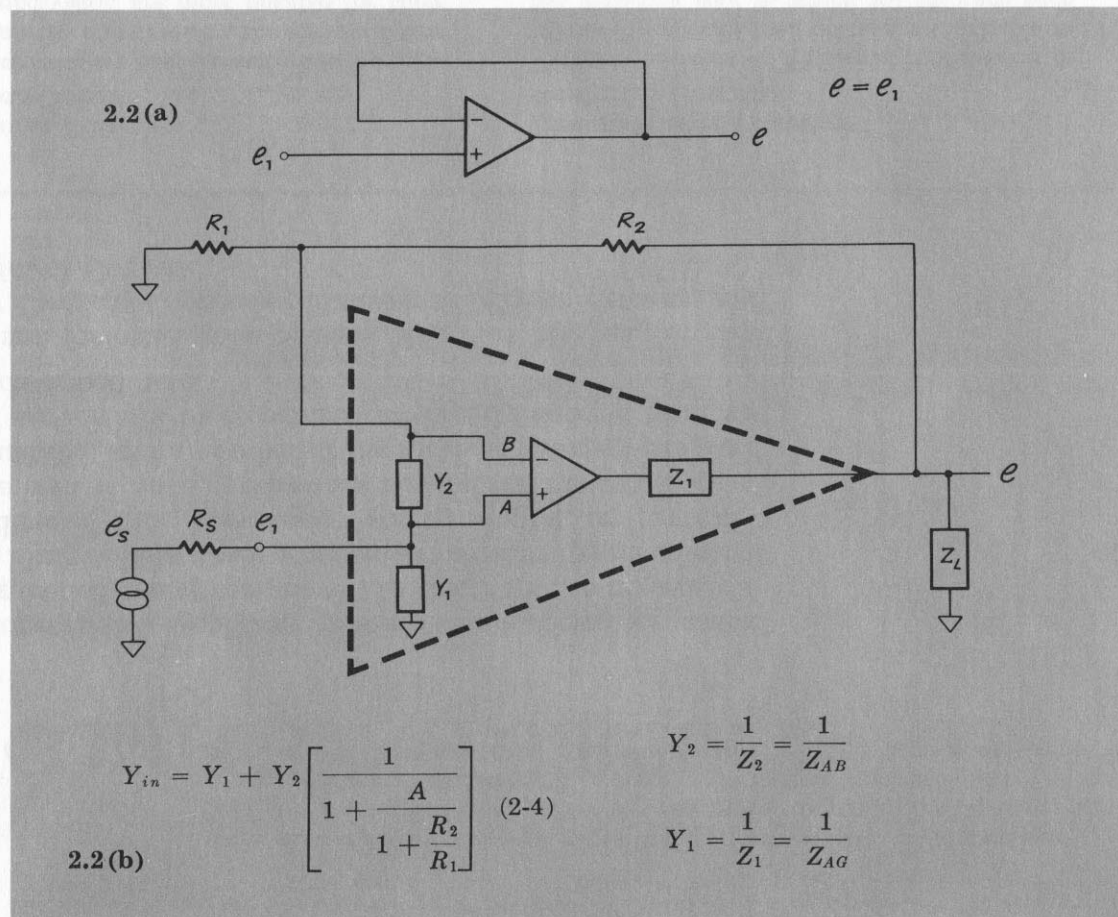
The response of the follower-with-gain circuit (b) is

$$e = \left(1 + \frac{R_2}{R_1}\right) e_1 \quad (2-3)$$

Circuit (b) is less demanding of differential excellence, for two reasons. First, for equal outputs, the input (i.e., common-mode) voltage of (b) is smaller. Thus, even a curvilinear relationship between common-mode error and common-mode voltage is correctable, in (b), by trimming gain, assuming the gain is high enough.

Secondly, some differential amplifiers have dynamics that are optimized for inverting work, and, therefore, respond more rapidly to signals applied to the negative input terminal than to the positive. For low values of gain, the positive-input lag rather than the gain-bandwidth product limits the speed of response. Also, output rate-limiting resulting from input saturation is much less a factor in (b), because of the smaller input. For these reasons an amplifier having severe limitations as a unity-gain follower may be excellent as a gain-of-100 follower-amplifier.

The input admittance of (b), for  $R_1$  or  $R_2 \ll 1/Y_2$ , is given in equation (2-4).



2.2(b)

$$Y_{in} = Y_1 + Y_2 \left[ \frac{1}{1 + \frac{A}{1 + \frac{R_2}{R_1}}} \right] \quad (2-4)$$

$$Y_2 = \frac{1}{Z_2} = \frac{1}{Z_{AB}}$$

$$Y_1 = \frac{1}{Z_1} = \frac{1}{Z_{AG}}$$

II.2  
I.5  
to  
I.7  
I.16  
I.18  
I.23  
III.32  
to  
III.34

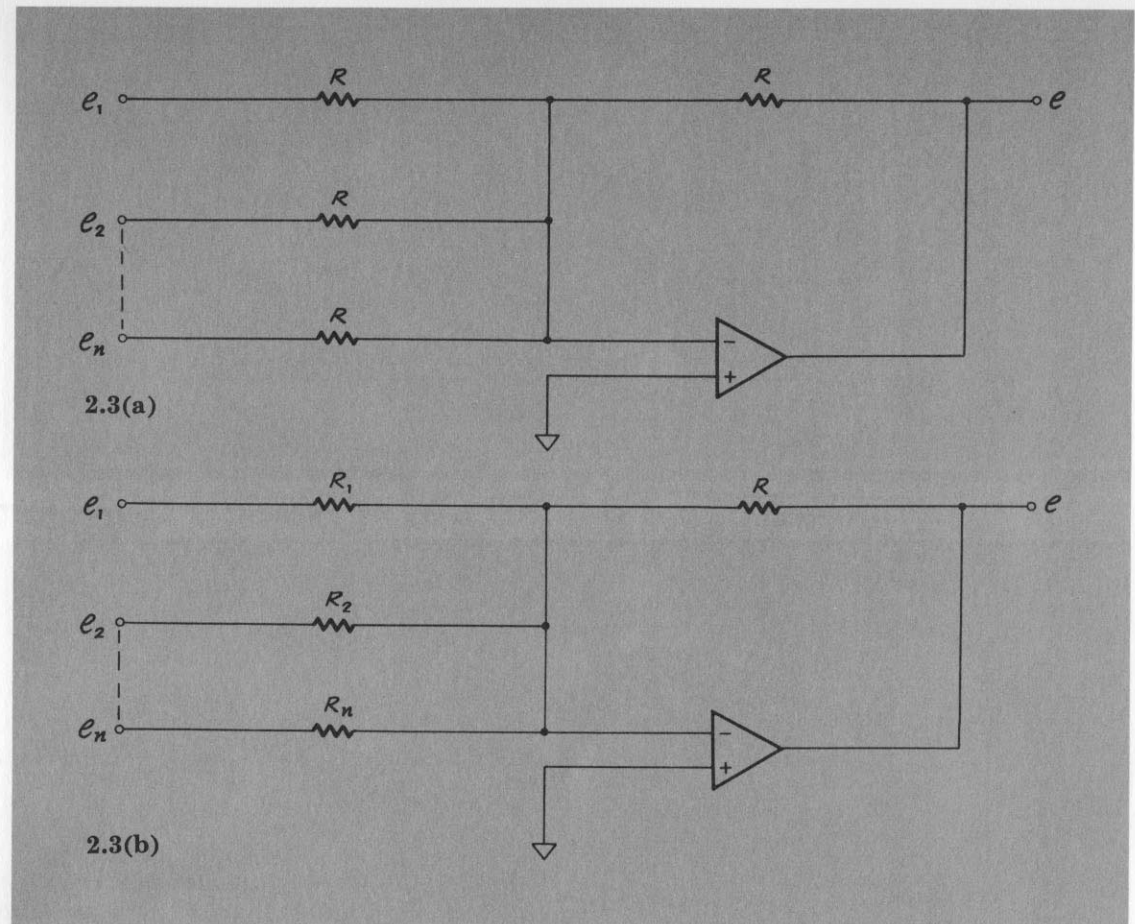


**II.3 THE INVERTING ADDER—WITH & WITHOUT WEIGHTING.** Circuit (a) adds linearly; that is, when  $n$  input voltage signals  $e_1, e_2, \dots, e_n$ , are applied to the input terminals, the voltage sum is delivered at the output terminal. (See I.7.) When all resistors are equal, the circuit thus acts as a one-to-one inverter with respect to each input to a very high accuracy provided that the amplifier gain is high. The response is given by:

$$-e = e_1 + e_2 + \dots + e_n \quad (2-5)$$

Circuit (a) is but a special case of the generalized circuit of section I.6, and it immediately suggests other circuits, less general than that of I.6, but more general than (a)—for example, (b), in which the individual input resistors may have values different from that of the feedback resistor, so that the output is the sum of a series of terms, each proportional to one of the input signals, *but each multiplied by an arbitrary coefficient*. Thus, in producing a “sum,” we may *weight* (or “scale”) the inputs arbitrarily, merely by selecting appropriate values of input resistance. Circuit (b) is sometimes called a “Linear Combinor.” Its response is given by:

$$-e = e_1 \left( \frac{R}{R_1} \right) + e_2 \left( \frac{R}{R_2} \right) + \dots + e_n \left( \frac{R}{R_n} \right) \quad (2-6)$$



**II.4 THE NON-INVERTING ADDER.** The output of this circuit is (ideally) the direct, *positive* sum of the two inputs. In other words, we have constructed a *non-inverting* adder. A brief analysis of this circuit should prove useful, since its fundamental configuration permits a number of interesting variations.

As always, we begin by assuming that  $e_n$  is 0, so that the potential with respect to ground at the positive input,  $e_A$ , is the same as that at the negative input,  $e_B$ . From the proportions of the feedback network connected to the negative input, it is clear that:

$$e_B = e \left( \frac{R}{R + R} \right) = \frac{e}{2} \quad (2-7)$$

We may also derive an expression for  $e_A$ , in terms of  $e_1, e_2$ , and the resistance values.

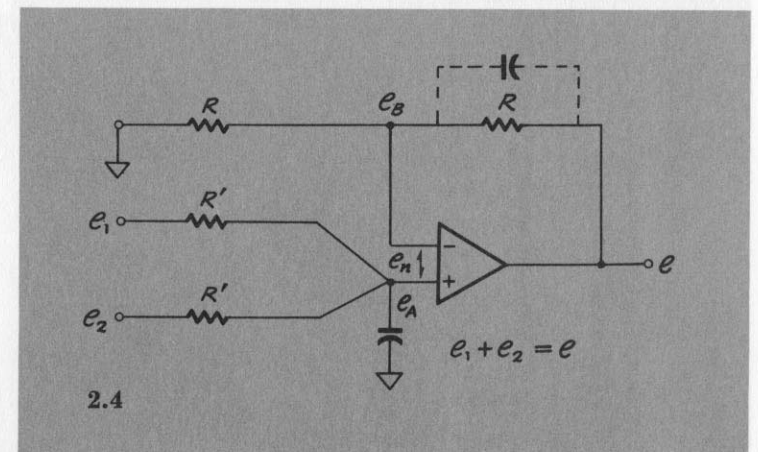
$$\frac{e_1 - e_A}{R'} + \frac{e_2 - e_A}{R'} = 0 \quad (2-8)$$

$$e_1 + e_2 = 2e_A \quad \text{or} \quad e_A = \frac{(e_1 + e_2)}{2}$$

If the input-terminal potentials are equal,

$$e_A = \frac{e_1 + e_2}{2} = e_B = \frac{e}{2} \quad \text{or,} \quad e_1 + e_2 = e \quad (2-9)$$

This circuit is not limited to two inputs, nor to *simple* addition—the coefficients may be arbitrarily weighted by using appropriate resistor values and some algebra.



II.3  
I.5  
to  
I.7  
I.18  
II.4  
to  
II.10  
II.19  
II.23

II.4  
I.5  
to  
I.7  
I.16  
I.18  
II.3  
II.5

**II.5 THE NON-INVERTING ADDER/SUBTRACTOR.** Only a perverse and unnatural insensitivity could resist exploring the possibility of obtaining *negative coefficients* with some practical form of the preceding circuit, and thus achieving *subtraction* . . . preferably, of course, without compromising the ability of the circuit to add, simultaneously. Circuit (a) satisfies both ambitions. Space does not permit the derivation of the expression for the output voltage, but it can be shown that, *provided that* the following relationship is satisfied:

$$k_1 + k_2 + k_3 = k_4 + k_5 \quad (2-10)$$

the response equation is given by:

$$e = k_4 e_4 + k_5 e_5 - (k_1 e_1 + k_2 e_2 + k_3 e_3) \quad (2-11)$$

A simple way of “forcing” the provisional relationship is to add a resistor,  $R/k_0$  or  $R'/k_0$ , from either the negative terminal of the amplifier or the positive terminal, to ground, depending upon which side of the provisional equation must be made larger to achieve the equality. This resistor, since it is grounded, corresponds to a term of the general form:  $k_0 e_0$  in which the voltage,  $e_0$ , is zero, and hence does not add a signal term to the basic rela-

tionship. If a single input,  $e_1$ , is applied to the negative terminal, and a single input,  $e_2$ , is applied to the positive terminal, and  $k_1 = k_2 = 1$ , then the circuit is reduced to a simple subtractor, figure (b), the response of which is:

$$e = e_2 - e_1 \quad (2-12)$$

It should be noted that, in this as well as in the circuit of Figure 2.4, the input resistors indicated are each assumed to *include* the resistance of their voltage sources; indeed, this is always assumed in circuits in which an input resistor is shown connected to an ideal zero impedance source.

There is no theoretical restriction on the number of input paths that may be added to either side of this circuit. If there are “m” inputs to the negative-terminal summing point and “n” to positive-terminal summing point, as in figure (c), the general expression for response is:

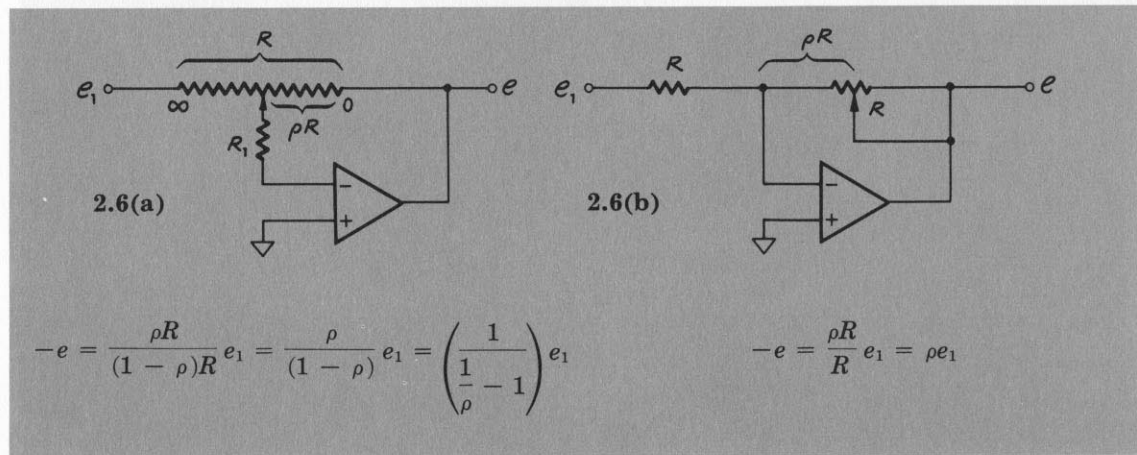
$$e = \sum_{j=1}^n k_j' e_j' - \sum_{i=1}^m k_i e_i \quad (2-13)$$

provided that:

$$\sum_{j=1}^n k_j' = \sum_{i=1}^m k_i \quad (2-14)$$

**II.6 ADJUSTABLE-COEFFICIENT INVERTERS.** In circuit (a) we have the true “adjustable electronic lever” with the tap of the potentiometer providing the adjustable “fulcrum.” This results in a wide-range, variable-gain amplifier that may be precisely, if not conveniently, calibrated. A voltage gain of  $-1$  occurs at mid-setting, while gains from a precise zero to very high values are within range. Note that a relatively small resistor,  $R_1$ , serves to protect the amplifier and prevent overload of the input source when  $\rho$  approaches unity. Note also that signal source impedance will generally affect the accuracy of the equation and limit the maximum gain.

If the potentiometer is placed in the feedback path alone, as in circuit (b), a proportioning device is obtained with narrower range than that of a circuit (a) but having a linear scale with respect to potentiometer rotation—a greater convenience, at times.



$$-e = \frac{\rho R}{(1 - \rho)R} e_1 = \frac{\rho}{(1 - \rho)} e_1 = \left( \frac{1}{\frac{1}{\rho} - 1} \right) e_1$$

$$-e = \frac{\rho R}{R} e_1 = \rho e_1$$

II.5  
I.5  
to  
I.7  
I.16  
I.18  
II.3  
II.4  
III.39  
III.81

II.6  
I.35  
II.1  
II.3  
II.7  
II.8



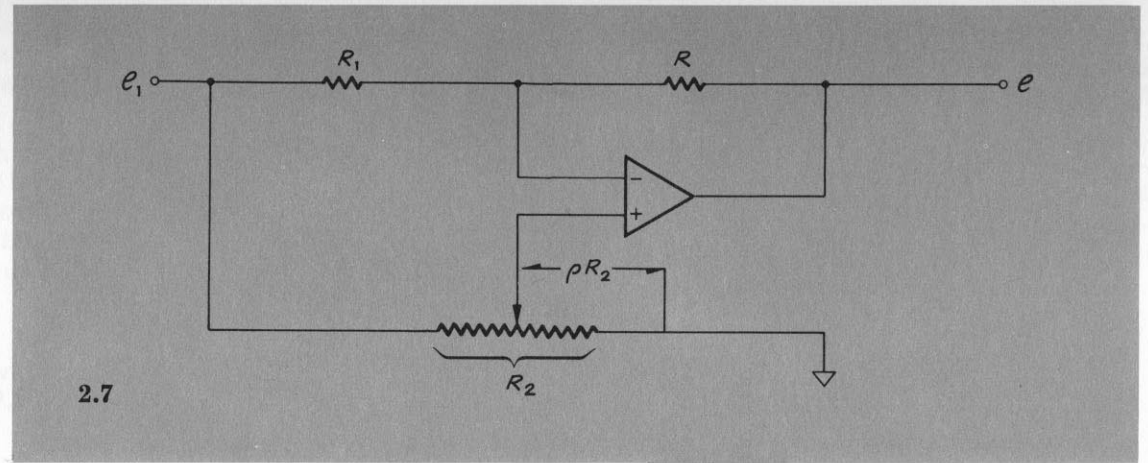
## II.7 BIPOLAR ADJUSTABLE-COEFFICIENT CIRCUIT.

It is but a short step from the end of II.6 to a circuit that draws upon the adder/subtractor technique to provide a wide and continuous range of coefficient adjustability, from a substantial negative value, through zero, to a substantial positive value. In the circuit shown, if  $R = R_1$ , the response varies between +1 and -1, linearly with rotation, passing through zero at  $\rho = 0.5$ . The relationship between  $\rho$  and the response is: (for  $R = R_1$ )

$$e = (2\rho - 1)e_1 \quad (2-15)$$

Note that this useful circuit may be given a different upper-limit coefficient, by adjusting the ratio of  $R$  to  $R_1$ . The general expression for the response is:

$$e = \left[ \left( 1 + \frac{R}{R_1} \right) \rho - \frac{R}{R_1} \right] e_1 \quad (2-16)$$



2.7

II.7  
I.35  
II.1  
II.6  
II.8  
II.9

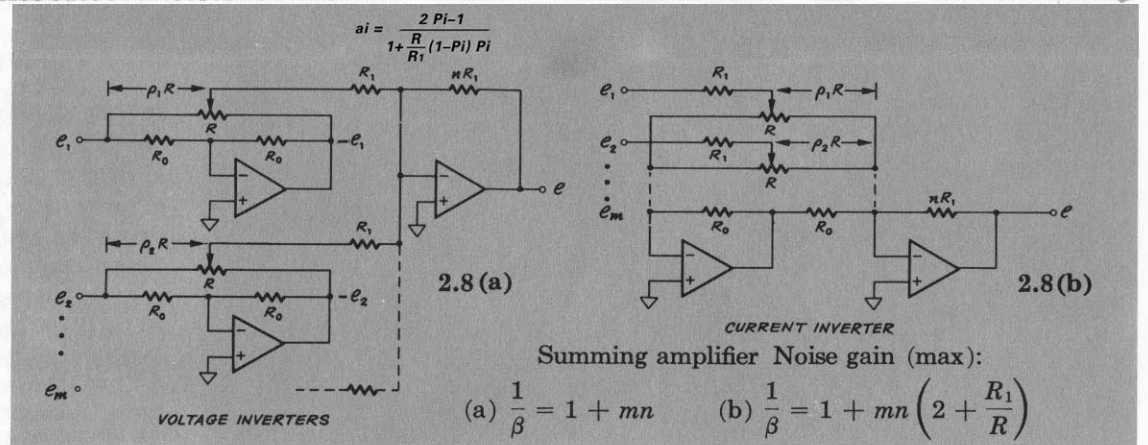
**II.8 BIPOLAR ADJUSTABLE-SCALE COMBINOR.** The circuits (a) and (b) perform identical mathematical operations.

$$e = n(a_1e_1 + a_2e_2 + \dots + a_me_m) \quad (2-27)$$

Circuit (a) requires more amplifiers but these can be inexpensive types, since the circuit impedance level,  $R$ , is arbitrary.

Circuit (b) requires only two amplifiers. They are generally selected so as to have nearly equal performance, because their error contributions tend to be identical. Furthermore, the noise gain ( $1/\beta$ ) of the main amplifier of (b) is twice that of (a) if the current inverter is scaled so that it just avoids saturation (i.e.,  $R_0 = R_1/m$ ).

The noise gain of (b) is minimized by using large values of  $R$ , while (a) permits use of the lowest feasible values of  $R$ .



Summing amplifier Noise gain (max):  
(a)  $\frac{1}{\beta} = 1 + mn$  (b)  $\frac{1}{\beta} = 1 + mn \left( 2 + \frac{R_1}{R} \right)$

II.8  
I.35  
II.1  
II.3  
to  
II.7  
II.9

**II.9 THE WEIGHTED AVERAGER.** A special case of the Inverting Adder, or Linear Combinor (II.3), this circuit uses matching resistors in a voltage-dividing network that assures that the sum of the weighting coefficients is always precisely unity. The Weighted Averager yields an output that is the (inverted) weighted average of the inputs.

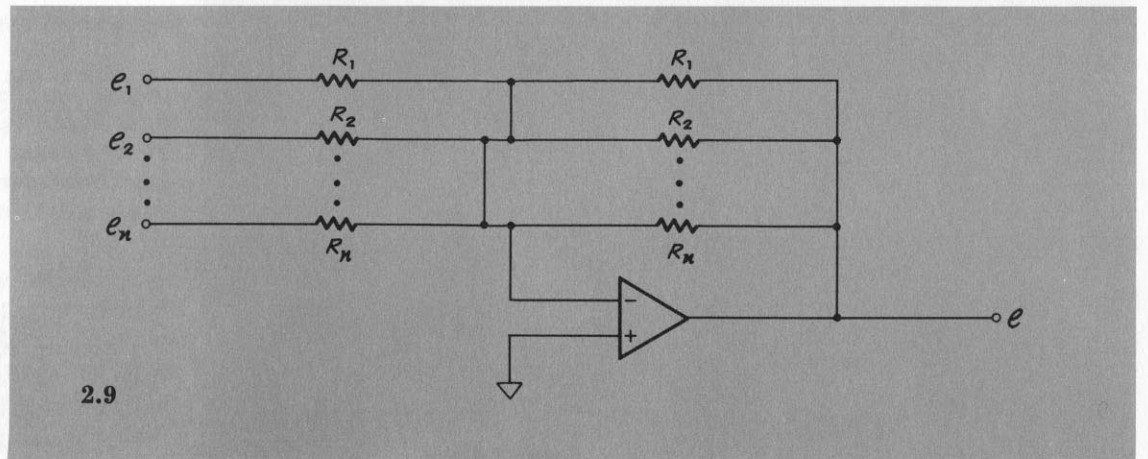
$$-e = a_1e_1 + a_2e_2 + \dots + a_ne_n$$

where

$$a_k = \frac{1/R_k}{\frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_n}} \quad (2-18)$$

and where

$$a_1 + a_2 + \dots + a_n = 1$$



2.9

II.9  
II.1  
II.3

**II.10 SINGLE-INPUT AND SUMMING INTEGRATORS.** The ability to integrate accurately is of fundamental importance in solving differential equations and modelling dynamic systems. The circuit of Figure (a) shows a simple running integrator (no reset or hold logic) that can be used within a stable feedback loop. In this circuit, in the ideal case, all the current flowing through the input resistor,  $e_1/R$ , must flow through the feedback capacitor. Hence:

$$-C \frac{de}{dt} = \frac{e_1}{R}$$

and thus

$$e = -\frac{1}{RC} \int^t e_1 dt \quad (2-19)$$

The *characteristic time* of the integrator is  $T = RC$ . (For example:  $R = 1$  megohm,  $C = 1 \mu F$ ;  $RC = 1$  sec.) This is the time required for the output to change by an amount equal to the average value of the input,

$$-\Delta e = \frac{\Delta t}{RC} \bar{e}_1 \quad (2-20)$$

A very long characteristic time can be achieved by using a TEE network (I.26) of resistors in place of the input resistor, and a large, low-leakage feedback capacitor. For example, a  $10 \mu F$  polystyrene capacitor, together with an effective 100 megohm TEE network, gives a 1000-second ( $16\frac{2}{3}$  min.) characteristic time. In this example, the amplifier offset current must be low, since even 10 pA of offset produces an error equivalent to that caused by 1 mV of voltage offset. On the other hand, the capacitor leakage resistance may become the dominant error factor, since it must exceed  $10^{12}$  ohms, at 10 volts of output, for the leakage current to be less than 10 pA.

For high-speed operation, a 1 m sec. time constant ( $R = 10$  k $\Omega$ ,  $C = 0.1 \mu F$ ) may be taken as typical. In this case, leakage current is not of great concern unless there is to be a long "hold." (See II.12, III.57.)

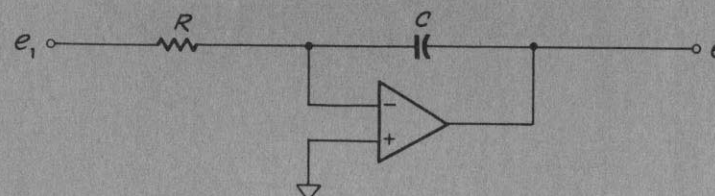
**II.11 THE AUGMENTING INTEGRATOR.** When a resistance,  $R_0$ , is placed in series with the feedback capacitor of an integrator, the circuit will produce a composite output, containing a component proportional to the input signal, added to a component proportional to the *time-integral* of the input signal.

This circuit has applications in closed-loop controllers (to provide a proportional-plus-reset control action) as well as in the simulation of many commonly-encountered physical systems. It is adaptable to summing and differential integrators, too, with and without weighting. By adding  $R_0$  in series with  $C$  in 2.10 (b), for example, we create a response given by:

$$-e = \frac{R_0}{R} \left( 1 + \frac{1}{T_p} \right) (e_1 + e_2 + \dots + e_n) \quad (2-21)$$

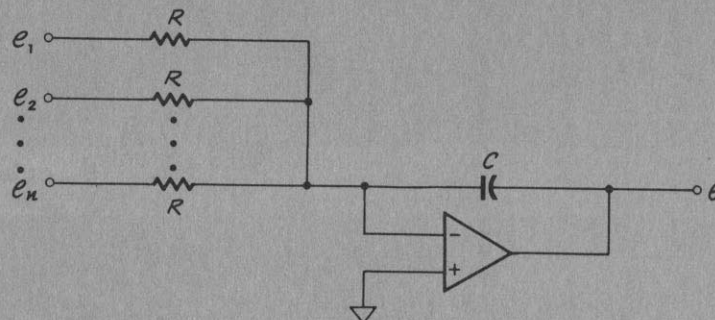
where

$$T = R_0 C$$



2.10(a)

$$-e = \frac{1}{T} \int^t e_1 dt \equiv \frac{1}{T_p} e_1$$

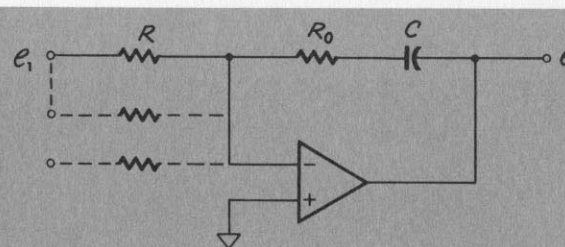


2.10(b)

$$-e = \frac{1}{T} \int^t (e_1 + e_2 + e_3 + \dots + e_n) dt$$

$$T = RC$$

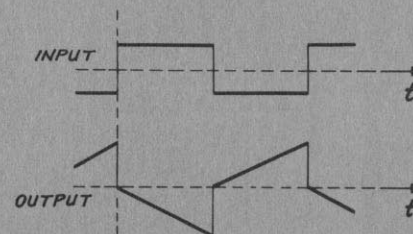
Adding more inputs to achieve a summing integrator is illustrated in (b). By choosing unequal input-resistor values, the contributions to the output (integral) of the several inputs may be weighted, in direct proportion to their conductance.



2.11(a)

$$-e = \frac{R_0}{R} \left( 1 + \frac{1}{R_0 C_p} \right) e_1$$

2.11(b)



II.10  
I.6  
II.12

II.11  
I.6  
II.10  
II.12



## II.12 PRACTICAL CONSIDERATIONS IN INTEGRATOR DESIGN.

The free-running-integrator circuit of II.10 must be used within a stable feedback loop, because it contains no inherent provisions for forcing it to an arbitrary output (initial) condition at an arbitrary time (time zero) . . . and an open-loop free-running integrator will, in time, drift to one of its bounds.

The most common way to impose an arbitrary initial condition upon an open-loop integrator is to use a relay circuit, such as (a). (See also II.49, II.50, and II.51.) Externally-generated logic signals are then used to control the mode—*run*, *set*, or *hold*. Figure (b) shows a typical output history. During each *set* mode interval, the integrator output relaxes to  $E_{I.C.}$  in accordance with:

$$e = E_{I.C.} + (e_s - E_{I.C.})e^{-\frac{t}{R_B C}} \quad (2-22)$$

where  $e_s$  is the value of  $e$  at the start of the *set* interval. The *set* interval must last long enough to allow the transient to subside ( $7R_B C$ , for 0.1% accuracy). For fast reset,  $R_B$  should be very low.\*

If current through  $R_A$  must be avoided, one may use two amplifiers, resetting the integrator to a zero initial condition ( $R_A$  "infinite"), and then, as shown in (c), adding the arbitrary initial condition in a separate summing amplifier. Note that in (c), because  $R_B$  is very small, one cannot ground the back contact of the *set* relay, as is done in (a), to minimize relay leakage current during the *run* and *hold* modes. In (c), one can attenuate in  $A$  and amplify in  $B$ , scaling the circuits so as to impose any arbitrary full-scale initial condition (within the ratings of  $B$ ) without saturating  $A$ .

When switching from *set* to *run*, it is necessary to avoid having both relays of circuit (a) closed at the same time, lest an error (indicated by dashed lines at the right of the history graph), be introduced. This error can be avoided by going through an intermediate *hold* state, also indicated in Figure (b), possibly at the expense of control-logic simplicity. (The *hold* state is a logical requirement in some systems, anyway.)

When several integrators are involved in a simulation, errors may be introduced if they do not all switch modes simultaneously. These errors are small if the characteristic time is large compared to relay-closure time differences.

In the *hold* mode, the output will tend to drift at a rate  $\bar{I}/C$ , where  $\bar{I}$  represents the average sum of all unwanted currents.

Hence, it would appear that the larger the capacitance (for a given total leakage current) the better. However, practical capacitors have a leakage conductance directly proportional to capacitance. When great care has been taken to minimize all other sources of leakage, such as amplifier input current and relay insulation, no substantial improvement in drift rate is possible by using a high quality (polystyrene) capacitor greater than  $1 \mu F$ .

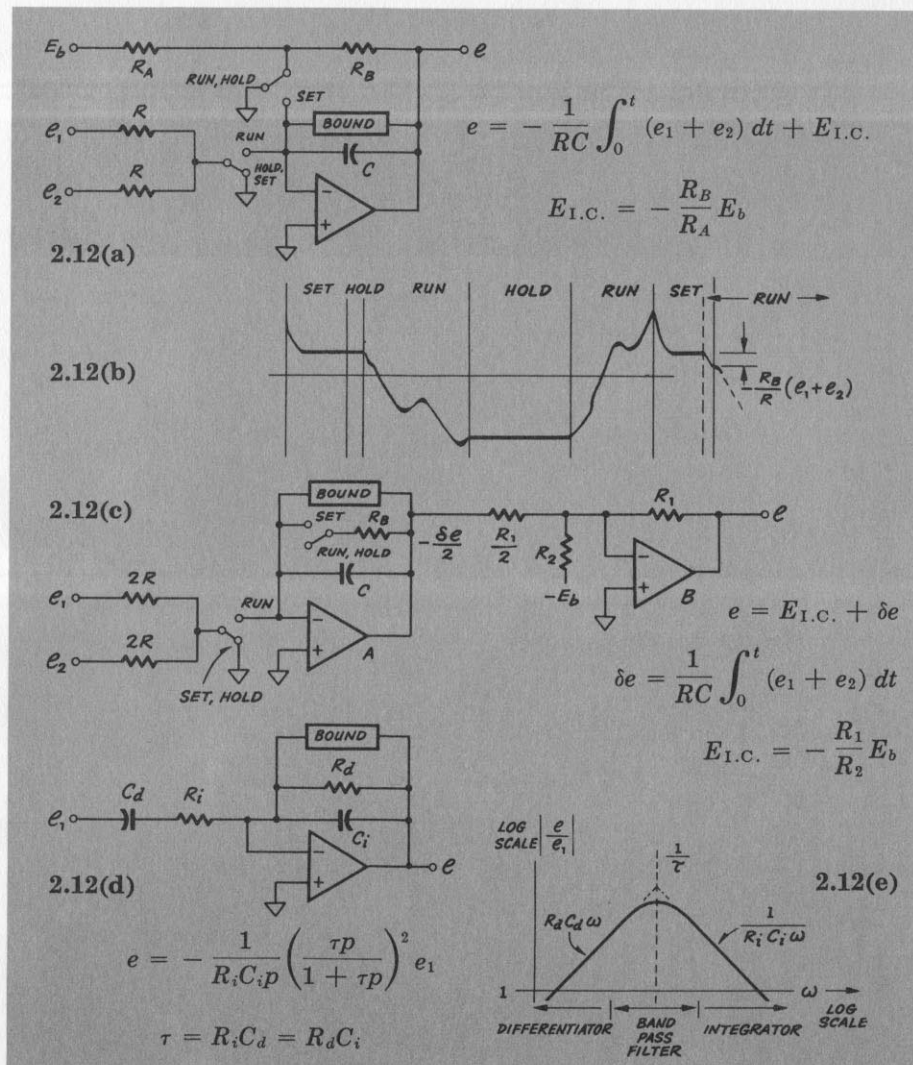
In the *run* mode, another source of drift appears. The amplifier offset voltage drives, through the sum of all input admittances, an additional error current. Thus, for minimum drift in the *run* mode, an amplifier with both low offset current and low offset voltage is required. In the *hold* mode, as noted, only offset current must be minimized, assuming that the amplifier's input resistance

is sufficiently high to minimize the error current due to voltage offset.

If there is a possibility that the amplifier output voltage range may be exceeded, a feedback-circuit bound is desirable. This enables the integrator to respond immediately if the net input changes sign. By properly guarding the bound (see I.25) leakage can be made less than  $10^{-12} A$ .

Instead of relay resetting, AC coupling, as in (d), can be used to prevent integrator runaway. (See also III.73.) Depending upon the frequency range of interest, this circuit can serve as a differentiator (at low frequencies), a band-pass filter (at mid-frequencies), or an integrator at high frequencies. It is usually best to set:

$$R_i C_d = R_d C_i \quad (2-23)$$



II.12  
I.6  
I.7  
I.11  
I.12  
I.13  
I.14  
I.18  
I.25  
I.33  
I.36  
II.10  
II.11  
II.13  
II.14  
II.21  
II.49  
II.50  
II.51  
III.27  
III.46  
III.57  
III.73

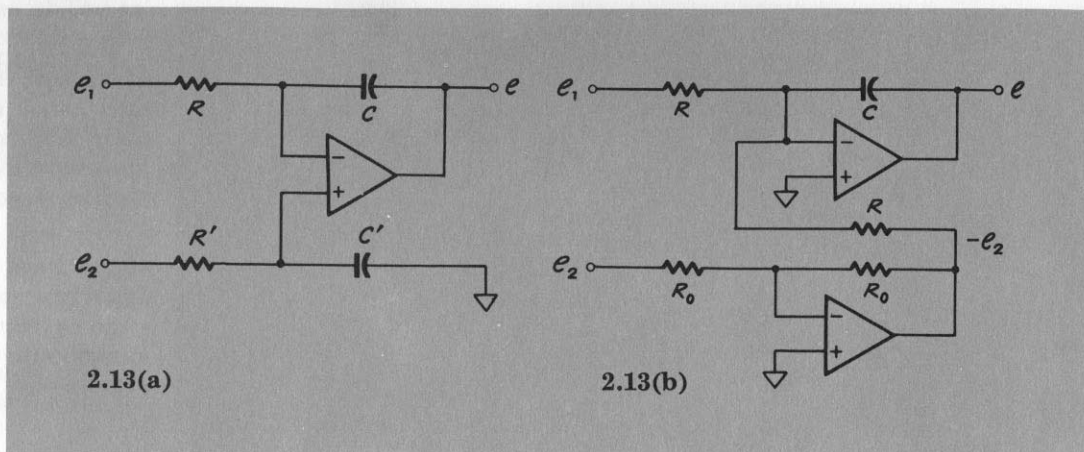
\*To protect the relay contacts,  $R_B$  must be at least 10–100  $\Omega$ .

**II.13 THE DIFFERENCE INTEGRATOR.** Having gone this far, it takes little daring, we submit, to replace two of the resistors in the adder-subtractor of II.5 with capacitors, thus creating the circuit shown here, in which the output is, at every moment, proportional to the time-integral of the difference between two signals.

If  $RC = R'C'$ , the input-output relationship is simplest:

$$e = \frac{1}{T} \int^t (e_2 - e_1) dt \quad (2-24)$$

Because two capacitors are used, the set-run-hold problems outlined in II.12 are compounded in the differential circuit of (a). Hence, circuit (a) is happiest in applications in which the loop is closed externally. Please note that an inverter and a summing integrator will do a similar job, as shown in (b).



2.13(a)

2.13(b)

**II.14 DOUBLE INTEGRATOR.** This extension of the basic integrator of II.10 permits a single amplifier to generate the second time-integral of an input signal. It is sometimes useful in handling dynamic system equations such as:

$$\frac{d^2x}{dt^2} + ax = f(t) \quad (2-25)$$

The response of this circuit is given by:

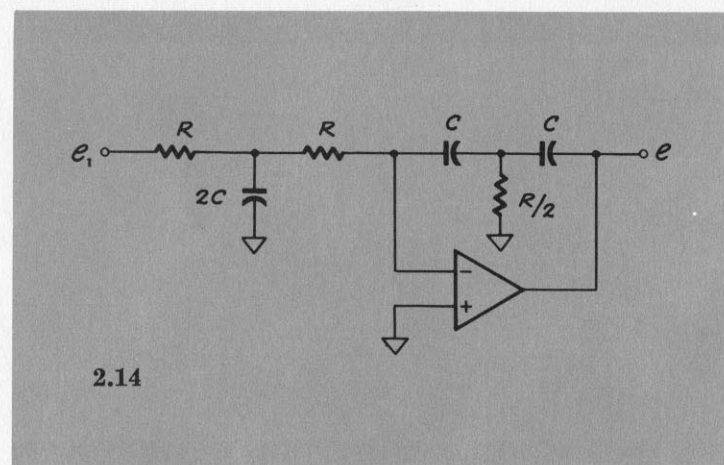
$$-e = \frac{1}{R^2 C^2 p^2} e_1 = \frac{1}{(Tp)^2} e_1 \quad (2-26)$$

where  $T = RC$

If the output is connected back to the input, this circuit will oscillate at a frequency given by:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi T} \quad (2-27)$$

When this circuit is connected as an oscillator, it is desirable, in practice, to modify the time-constants so that the feedback time constant is slightly shorter, and the input time constant is correspondingly longer, ensuring regenerative damping and (hence) buildup.



2.14

**II.15 SIMPLE LAG.** After a delay equal to many time constants ( $t \gg RC$ ) this circuit, in response to a "step" input at  $e_1$ , settles down to behave like any other arbitrary-coefficient inverter, approaching the familiar response of:

$$e = -\left(\frac{R}{R_1}\right) e_1 \quad (2-28)$$

Initially, however, it behaves like an integrator, and then its output exponentially approaches the inverter response at steady state. The net effect is to *delay* the appearance of the above-stated response . . . it "lags" the appearance of the input. This is called performing a "tardigrade" operation on  $e_1(t)$ .  $e_1$  need not be a step function, of course; regardless of the

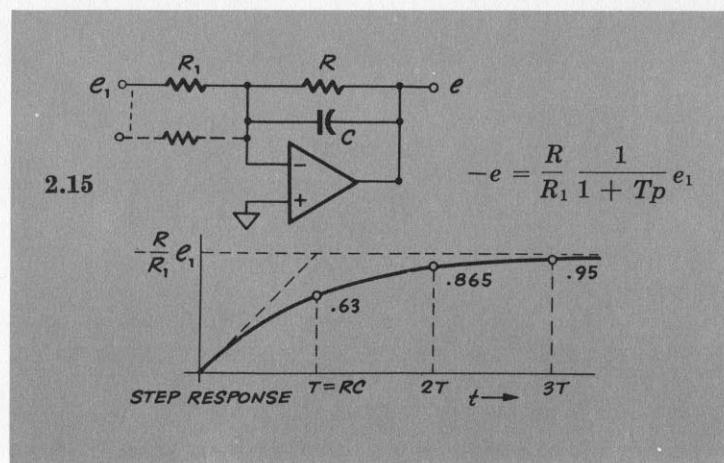
variation of  $e_1$  with time, the generalized response equation is:

$$-\frac{R}{R_1} e_1 = (1 + Tp)e \quad (2-29)$$

in operational notation, in which

$$pe \equiv \frac{de}{dt} \quad \text{and} \quad T = RC$$

Note that changing  $R$  affects both gain ( $R/R_1$ ) and time-constant ( $T$ ); while changing  $R_1$  affects only the gain. Note also that the lag may be applied to the *sum* of several inputs, as indicated in dashed lines, and weighting may be accomplished, also, by proportioning the input resistors.



2.15

$$-e = \frac{R}{R_1} \frac{1}{1 + Tp} e_1$$

II.13  
I.11  
to  
I.14  
I.18  
I.33  
II.10  
II.12  
III.12

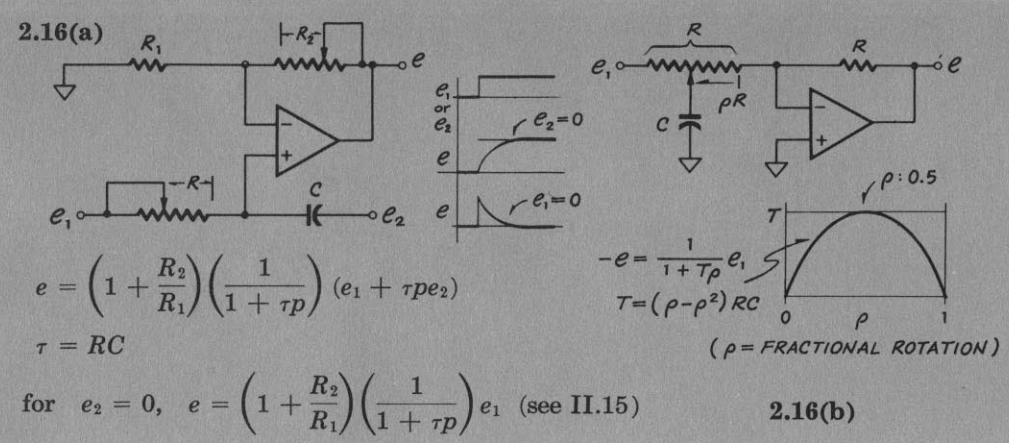
II.14  
I.6  
I.11  
to  
I.14  
I.18  
I.33  
II.10  
II.12  
III.10

II.15  
II.3  
II.10  
II.16  
III.54



**II.16 ADJUSTABLE-LAG CIRCUITS.** These two circuits permit continuous manual adjustment of the lag-response time constant, over a wide range. Circuit (a) provides independent adjustments of time constant and gain. The amplifier should have high CMRR; for long time constants, it must also have low input offset current. By driving the  $e_2$  input, a high-pass filter characteristic (imperfect differentiator) can be realized. Both  $e_1$  and  $e_2$  must be driven from low impedance (or grounded.)

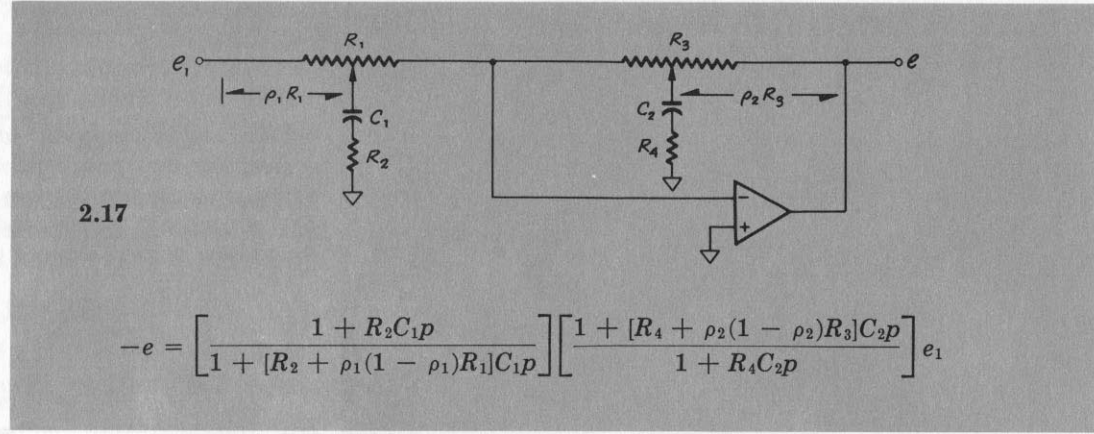
Circuit (b) is useful when inverting amplifiers must be employed, perhaps to gain the advantages of chopper stabilization; however, one must overcome the following drawbacks and inconveniences: dynamic instability at extreme settings; the general unavailability of high-resistance potentiometers; need for matching the feedback resistor to the potentiometer resistance.



II.16  
II.15  
II.17  
III.23  
III.26

**II.17 LAG-LEAD ELEMENT.** Introducing a lag into the feedback circuit (as well as into the input circuit, as was done in the preceding section) creates the possibility of a leading response, if the time constant in the feedback circuit is the greater of the two. If, as shown, we make both time-constants adjustable, we may arbitrarily change the response of the circuit from leading to lagging, merely by adjusting the time constants, relative to each other. When the time-constants are equal, the circuit becomes a unity-gain inverter.  $R_2$  and  $R_4$  insure dynamic stability.

This example illustrates a fairly general, yet flexible, configuration typical of many used for "lag-lead" compensation in instruments and controllers, and in the representation of thermal systems.

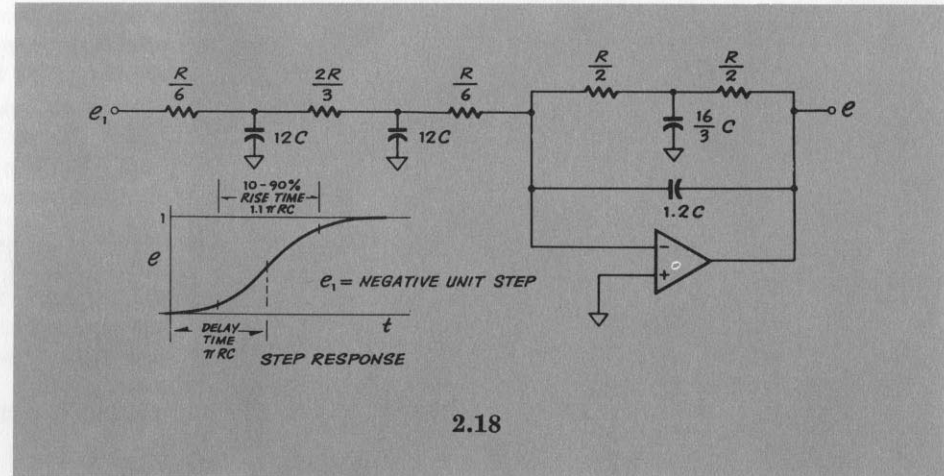


II.17  
II.15  
II.16

**II.18 DELAY-LINE ELEMENT.** This circuit is a third-order low-pass filter having phase lag nearly linear with frequency ( $\phi \propto \pi \omega RC$ ) in the range from 0 to 180°. In this sense, it approximates a delay,  $\exp(-\pi RCp)$ , although, unlike a pure delay, amplitude rolls off considerably  $\left( \left| \frac{e}{e_1} \right|_{\phi = 180^\circ} = \frac{1}{3} \right)$ . Amongst the merits of the circuit we may list the following: its transient-step response has no overshoot; its delay-time-to-rise-time ratio is nearly unity; and its first two derivatives are zero at zero time. The transfer operator is:

$$e = - \frac{1}{(1 + 2RCp)(1 + 1.2RCp + 1.6RCp^2)} e_1 \quad (2-30)$$

Note that there is a finite time delay before any appreciable response occurs, following which the response exhibits a rise time of the same order of magnitude as the delay. To improve the ratio of delay time to rise time, a number of stages ( $n$ ) may be cascaded; the ratio increases as  $\sqrt{n}$ .



II.18  
III.23  
III.24

**II.19 DIFFERENTIATOR.** Circuit (a) is of an “ideal” differentiator. The current into the summing point through  $C$  is:

$$i_c = C \frac{de_1}{dt} \quad (2-31)$$

and the feedback current, through  $R$ , must, in the ideal case, equal  $i_c$ , so that:

$$-e = i_c R = RC \frac{de_1}{dt} = T p e_1 \quad (2-32)$$

where  $T = RC$  and  $p e_1 = \frac{de_1}{dt}$

As we well know from earlier disillusionment, circuit (a) will not be dependably stable without at least a small feedback capacitor, like  $C_r$ .  $C_r$  is a good idea for at least one other reason: circuit (a) has a nasty preference (i.e., gain) for high-frequency noise, which tendency is much ameliorated by a gentle but firm roll-off above useful frequencies. Now, however, we no longer have a true differentiator;  $C_r$  has changed that.) (See II.21 for design consideration.)

Figure (b) shows that we may combine the derivatives of several signals in one Summing Differentiator. By now, this comes as no

surprise to any student of the fearful symmetry of nature—after all, we have already seen adders and summing integrators... why not summing differentiators? As might be expected, weighting of the individual derivatives is entirely practical, merely by proportioning the input capacitors. The ideal response equation for  $n$  inputs is:

$$-e = RC_1 p e_1 + RC_2 p e_2 + \cdots RC_n p e_n \quad (2-33)$$

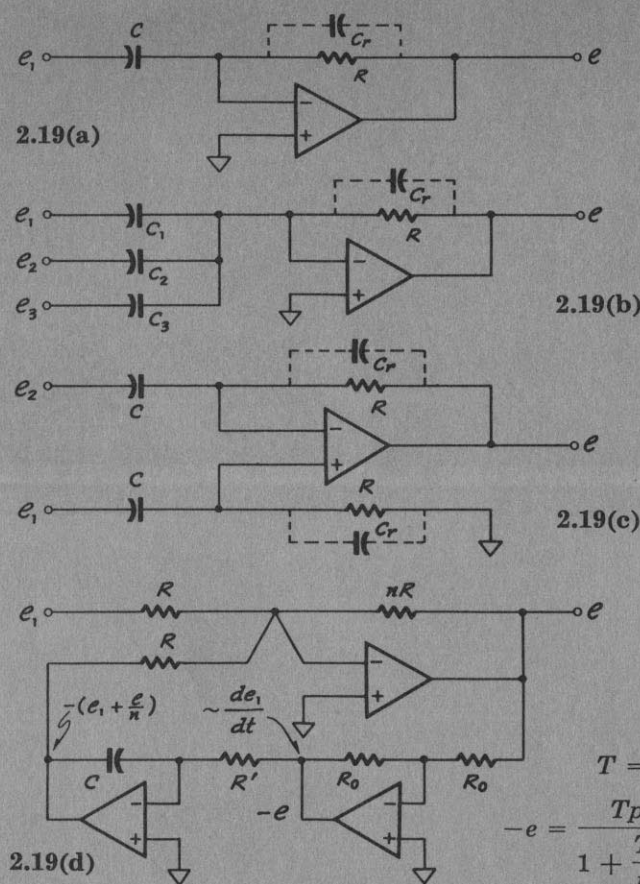
Figure (c) supports the theory of Harmony Throughout The Universe. It is a difference differentiator—that is, it produces an output proportional to the difference between two derivatives. For equal time-constants, the output expression is:

$$-e = T p (e_1 - e_2) \quad (2-34)$$

where

$$T = RC$$

Figure (d) shows a scheme that is commonly used in general-purpose analog computers. To maintain dynamic stability, one must not make  $n$  too large. In general, stabilizing this loop is more difficult than stabilizing the single-amplifier circuit 2.21 (b).

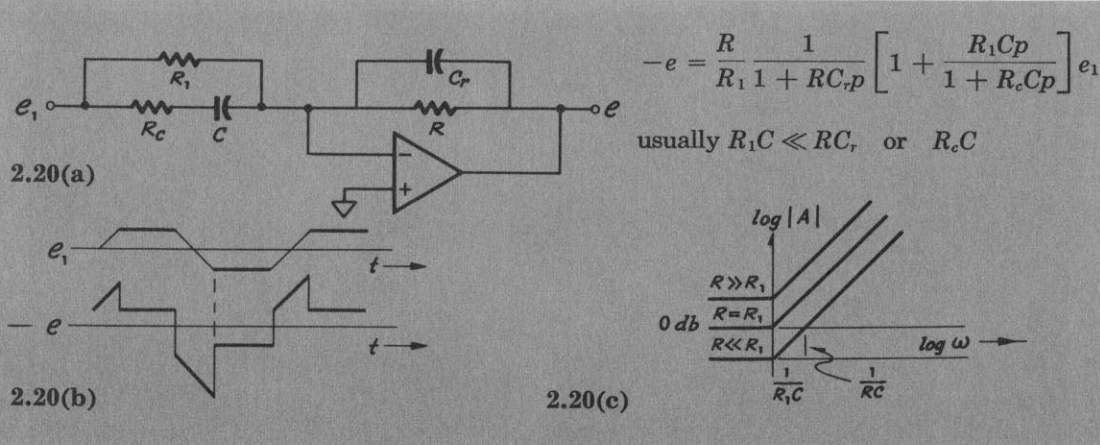


**II.20 THE AUGMENTING DIFFERENTIATOR.** The response of circuit (a) may be found by simple superposition, since the current contributions of  $R_1$  and  $C$  are independent because of the amplifier's summing property. The output voltage must furnish both currents, mainly through  $R$ , except at high frequencies above the useful differentiating bandwidth. The ideal response is given, therefore, to a good accuracy, by:

$$-e = \frac{R}{R_1} (1 + T p) e_1 \quad (2-35)$$

$$\text{where } T = R_1 C$$

and is illustrated in the exemplary graph of (b). The frequency response of this circuit is given in (c).



II.19  
I.6  
to  
I.14  
I.17  
I.42  
I.43  
II.20  
II.21

II.20  
II.11  
II.19  
II.21



## II.21 PRACTICAL CONSIDERATIONS IN DIFFERENTIATOR DESIGN.

In II.19 we mentioned the need for a small feedback capacitor to limit the gain at high frequencies and to provide dynamic stability. A further modification of the "ideal" differentiator circuit involves placing a small resistor in series with the input capacitor. This resistor also helps to limit the high frequency gain, and to ensure dynamic stability; furthermore it "cushions" the signal source by reducing the effective magnitude of the capacitive load seen at the input, and it limits the maximum input current. The addition of this resistor makes the practical differentiator circuit of (b) identical in form to the AC integrator circuit, Figure 2.12(d).

Circuit (b) is dynamically unstable (or at best marginally stable) if either  $R_i$  or  $C_i$  is absent, or if either is not high enough in value. To achieve well damped stability, the radian frequency,  $\omega_c (=1/\tau_c)$  should be chosen to be no greater than the geometric mean between  $\frac{1}{R_d C_d}$  and the amplifier's gain-bandwidth product,  $\omega_H$ . (See I.43.)

$$\tau_c > \sqrt{\frac{R_d C_d}{\omega_H}} \quad \text{or} \quad R_i C_i > \frac{1}{\omega_H} \quad (2-36)$$

Wisdom often dictates choosing a substantially larger value of  $\tau_c$  (than the geometric mean) in order to limit the sensitivity of the differentiator to high-frequency noise.

The differentiator characteristic time,  $R_d C_d$ , is selected so that the maximum rate of change of input signal will produce full-scale output. I.e., set

$$R_d C_d = \frac{|e|_{\max} \text{ (f.s.)}}{\left| \frac{de_1}{dt} \right|_{\max}} \quad (2-37)$$

Occasionally, a still faster (i.e., off-scale) input change may occur. The bound circuit shown in (b) will limit the output in that event, and prevent an erroneous charge from developing

across  $C_d$ . Thus protected from off-scale saturation, the output will respond correctly, even immediately following an anomalous steep transient.

For moderately-fast signals, choose  $R_d$  so that full-scale voltage across  $R_d$  develops between 0.1 and 1 milliamperes in it; however, if this computation calls for a (polystyrene) capacitor for  $C_d$  higher than 1 to 10  $\mu\text{F}$ , it is better (because of capacitor leakage) to limit the capacitor value to 10  $\mu\text{F}$ , and permit larger values of  $R_d$  in order to achieve a long enough characteristic time. In such a design, the full scale signal current will thereby be reduced, necessitating the selection of an amplifier with a correspondingly lower offset current rating, for accuracy, and higher input impedance, too. An exotic example of this procedure is given in III.56, which describes a differentiator design having a  $10^6$  second (nearly 2-week!) characteristic time.

The effective error produced by DC summing-point voltage and current offsets ( $E_0$  and  $I_0$ ) referred to the input is:

$$\left( \frac{de_1}{dt} \right)_{\text{error}} = \frac{1}{C_d} \left[ \left( \frac{1}{R_d} + \frac{1}{R_{in}} \right) E_0 + I_0 \right] \quad (2-38)$$

where  $R_{in}$  is the amplifier's effective input resistance.

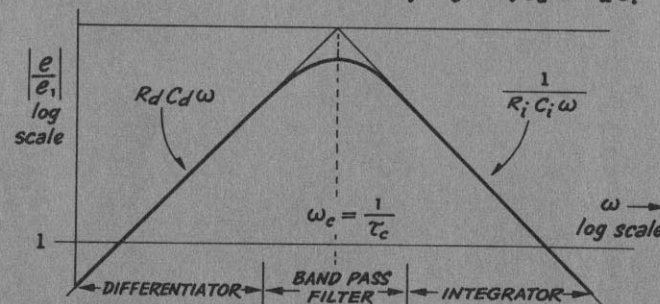
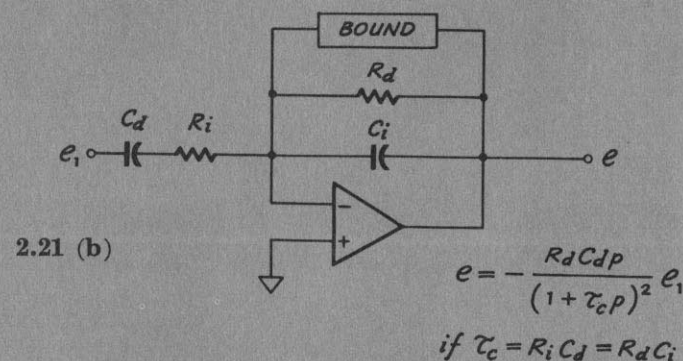
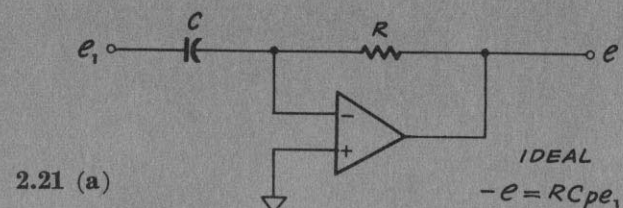
Choose the "critical" radian frequency:

$$\omega_c = \frac{1}{\tau_c} = \frac{1}{R_i C_d} = \frac{1}{R_d C_i} \quad (2-39)$$

as low as possible without causing excessive distortion (i.e., gain and phase error). The table (d) may prove helpful in assessing the gain and phase errors caused by the two lagging time constants  $R_i C_d$  and  $R_d C_i$ . Note that by substituting  $j\omega$  for the operator  $p$  in the input-output relation the gain and phase are given by:

$$- \left| \frac{e}{e_1} \right| = \frac{RC\omega}{1 + \tau_c^2 \omega^2} \quad (2-40)$$

$$\phi_{\text{lead}} = 90^\circ - 2 \tan^{-1} \tau_c \omega \quad (2-41)$$



$\omega \rightarrow$	$0.01 \omega_c$	$0.1 \omega_c$	$\omega_c$	$10 \omega_c$	$100 \omega_c$
MAGNITUDE ERROR*	NIL	-1%	-50%	-99%	-100%
PHASE ERROR*	-1.1°	-11.4°	-90°	-169°	-179°

\* departure from ideal

2.21 (d)

II.21  
I.5  
to  
I.14  
I.17  
I.18  
I.31  
I.42  
I.50  
I.51  
II.12  
II.19  
II.20  
III.56

**II.22 INHERENTLY NON-LINEAR ELEMENTS.** We have already seen (in I.32—DIODES) that certain semiconductor junctions exhibit a reasonably-accurate logarithmic relationship between voltage and current, over quite wide ranges of current. This *inherent* non-linearity is so useful, that many years have been devoted to the refinement of inherently logarithmic devices — searching out those that adhere with the greatest fidelity to the formula:

$$e = E_0 \log_{10} \left( \frac{i}{I_0} \right) \quad (2-42)$$

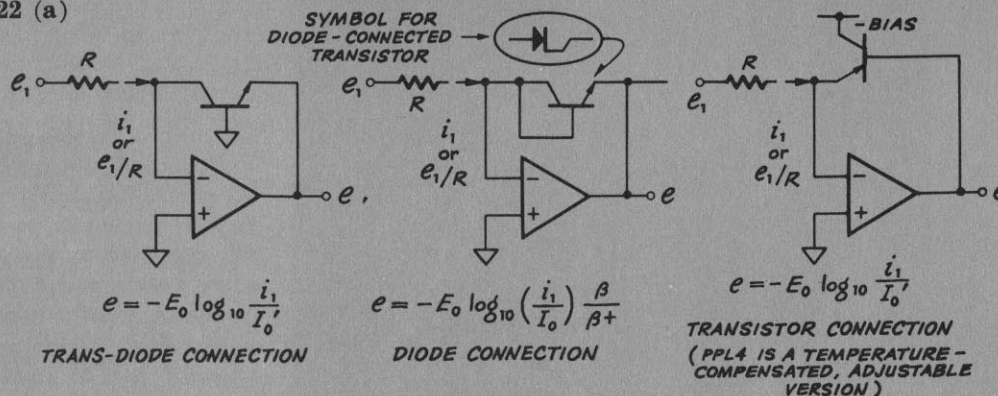
over the widest possible ranges of  $i$ , and then domesticating them ... by such means as temperature compensation, matching pairs, etc. These efforts have been crowned at Philbrick by the development of a family of devices known as LOGARITHMIC TRANSCONDUCTORS. The configurational versatility of typical members of this family is summarized briefly in Figure (a). Circuits (b) and (c) show the application (without temperature compensation) of just one form of these Transconductors to the generation of elementary log and anti-log functions. (See II.28–31 for fuller exposition.) The graph of Figure (d) shows the ranges over which the PL1/PPL1 transconductors adhere closely to the straight and narrow path.

Back in the dim past, it was not uncommon to use the more-or-less-square-law behavior of a vacuum-tube triode transfer characteristic to achieve quadratic nonlinearity; and the uses of nonlinear effects in vacuum tubes, transistors, capacitors, varistors, etc., still appear from time to time as preferred solutions to specific problems, in which compromises among functional fidelity, temperature sensitivity, and bandwidth are acceptable.

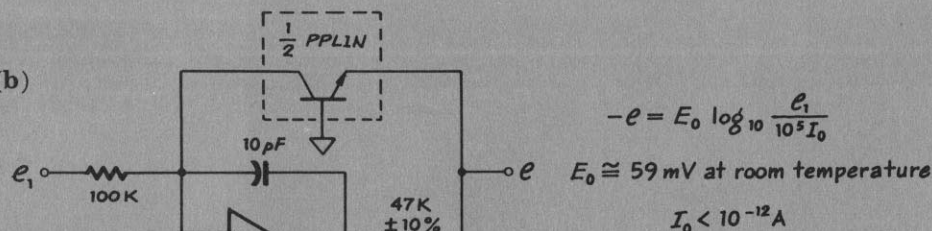
Specific recent examples include the multiplicative properties of field-effect transistors, and the clever use of silicon carbide for squaring in the Douglas Quadratron (now available from Bourns, Inc.).

Finally, no summary of inherently nonlinear elements for functional representation, however brief, would be complete without mention of the Hall effect. If any conductor carrying a current is placed in a transverse magnetic field, a voltage proportional to their true cross-product will appear across the conductor along the third axis. The constant of proportionality known as the *Hall Coefficient*, extremely small for most conductors, is appreciable in some recent devices. However, Hall-effect multipliers suffer from asymmetry and lack of common scaling, and they tend to be temperature-sensitive, but for many applications they are quite useful. Operational Amplifiers are used with Hall-effect devices for scaling, as current sources, and for field-driving.

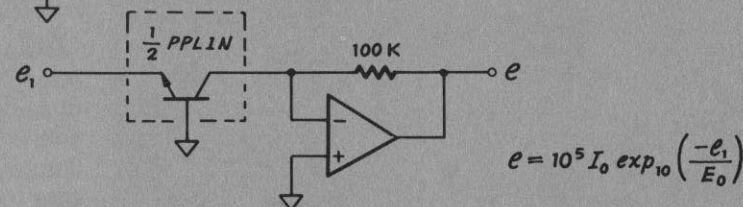
2.22 (a)



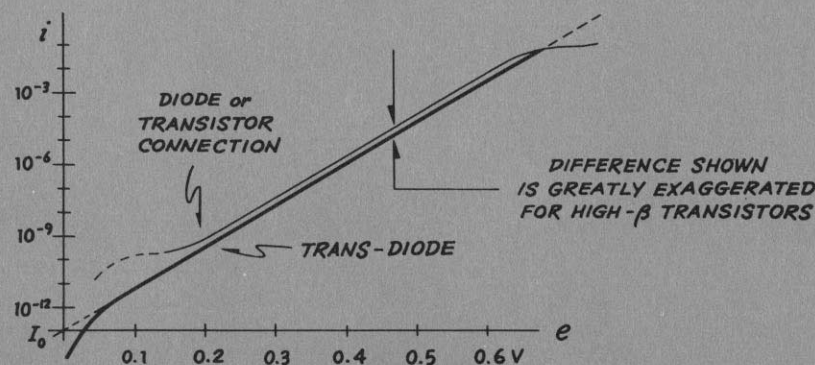
2.22 (b)



2.22 (c)



2.22 (d)



II.22  
I.32  
II.23  
to  
II.33  
III.45  
III.63  
III.64  
III.65  
III.68



**II.23 SYNTHESIZED-FUNCTION NON-LINEAR ELEMENTS.** Another fundamental way to create a known and dependably-reproducible nonlinear device is to construct a network, the elements of which are not in themselves selected for inherently-conformal nonlinear behavior, but which, when combined and proportioned appropriately, exhibit the desired nonlinear  $e/i$  relationship. Although such synthetic networks are invariably more ramified than are the inherently nonlinear devices, particularly if they must be very accurate, they offer far greater design freedom in the range and variety of available nonlinear functions. Time and toil have brought forth gratifyingly-accurate networks that exhibit logarithmic, transcendental, and quadratic behavior, and accommodate various combinations of voltage and current polarity. In their most convenient form, they appear as a family of Philbrick Operational Plugins, described briefly on the inside back cover of this manual, under the designations: PSQ-N/P, SPLOG-N/P, SPSIN-N/P, SPCOS-N/P, and SPFX-N/P. For the ultimate in flexibility, we commend to you the SK5-F.\* Circuit (a) is a simplified generic schematic of such a network. The graphical analysis (b) that accompanies it shows how such a network can be made to conform—at least grossly—to a particular arbitrary function. The input signal,  $e_1$ , is connected to  $n$  networks, each forming a divider between  $e_1$  and a negative reference voltage,  $E$ . Above some value of  $e_1$ , the diode will conduct, driving a current into the summing point. The necessary condition for diode conduction in the first branch is:

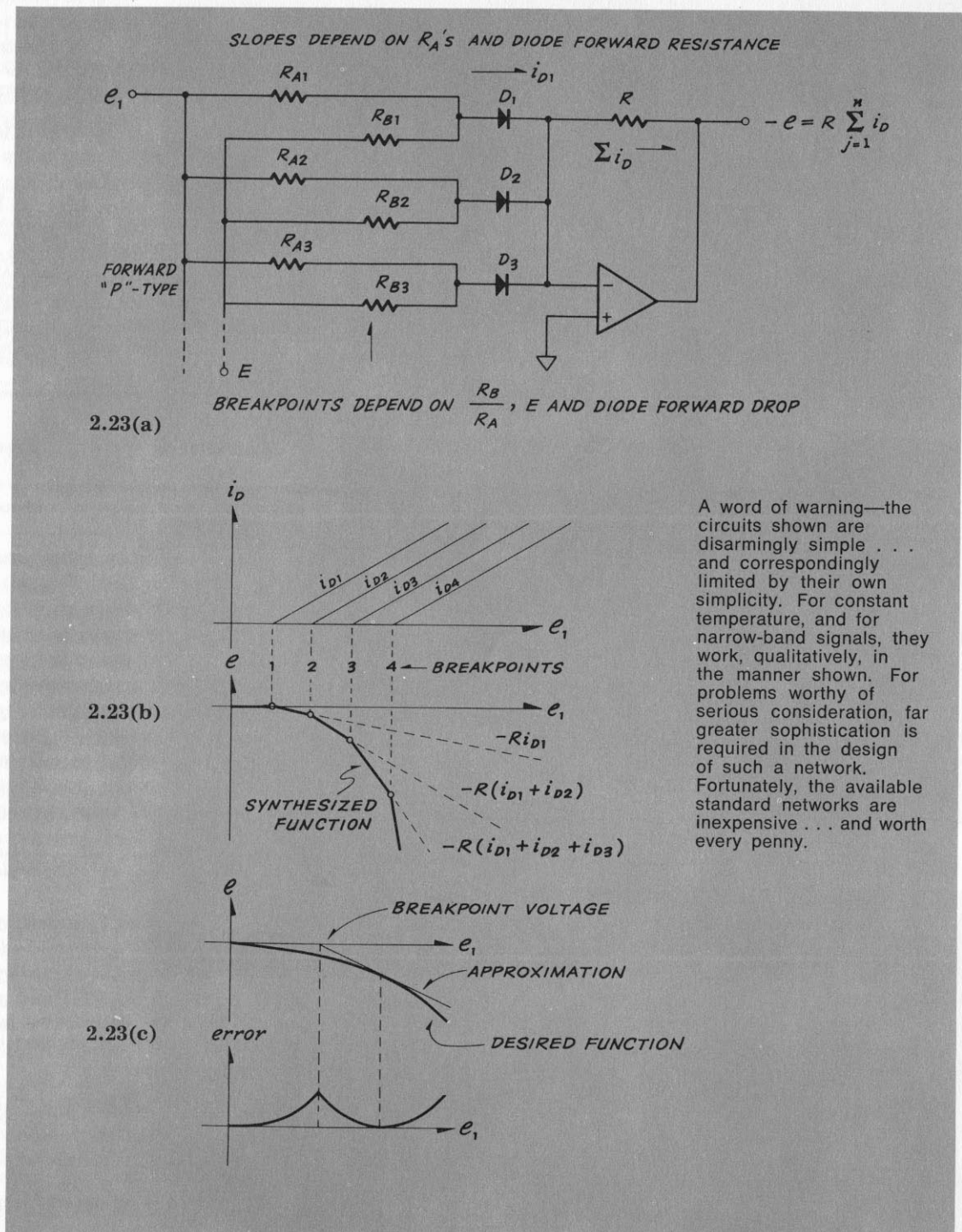
$$e_1 \geq \frac{R_{A1}}{R_{B1}} E \quad (2-43)$$

above which, the current that flows to the summing point (neglecting diode drop) is  $e_1/R_{A1}$ , since feedback from the amplifier (through  $R$ ) holds the summing point at a virtual ground (zero) potential. The complete expression for the current in  $D_1$ , then, is: (for  $i_{D1} > 0$ )

$$i_{D1} = \frac{\left(e_1 - \frac{R_{A1}}{R_{B1}} E\right)}{R_{A1}} = \left(\frac{e_1}{R_{A1}} - \frac{E}{R_{B1}}\right) \quad (2-44)$$

The difference between the desired function and the synthesized approximation is the systematic error of the device. Figure (c) shows such an error for an approximation made by line segments tangent to the desired function. Usually, these errors are expressed in percentage of full scale output. Use additional diodes (and associated reference voltages) connected in opposite polarity, and or additional amplifiers, to invert input voltages or computing currents if input voltages of opposite polarity are to be dealt with or non-monotonic functions to be embodied.

\*The SK5-F Manual should interest those who find this treatment of arbitrary nonlinearity intolerably brief.



II.23  
I.32  
I.34  
II.22  
II.24  
to  
II.33  
III.45  
III.63  
III.64  
III.65  
III.68

**II.24 BASIC CIRCUIT—LOG OR ROOT RESPONSE.** If we connect a nonlinear network (see 2.23(a)) so that the network is driven by the amplifier output and feeds back a current related to the voltage in a predictably-nonlinear manner, the response of the circuit will be:

$$e = -f^{-1}\left(\frac{e_{in}}{R}\right) \quad (2-45)$$

where  $f$  is the causal functional relationship between the voltage at A and the current into B. This circuit may be used to develop inverse functions. If, for example, we used Model PSQ-N (square-law characteristic), the response of the circuit connected for the inverse function (i.e., square root) would be:

**II.25 SQUARER.** Here we show a form of circuit 2.23(a), in which the nonlinear network is a PSQ-P Quadratic Transconductor, which has the basic  $e/i$  relationship:

$$i = \frac{1}{2} \times 10^{-3} \left(\frac{e_1}{10}\right)^2 = 5 \times 10^{-6} e_1^2 \quad (2-48)$$

When used as a squarer,  $e$  is connected to  $e_2$ . The output current of this network is then transduced to a voltage (see III.30), as described by the relationship:

$$e = -iR = \frac{e_1^2}{10} \left(\frac{R}{20 \text{ k}\Omega}\right) \quad (2-49)$$

The circuit as shown works only for positive values of  $e_1$ . If  $e_1$  is bipolar,  $-e_1$  should be

**II.26 ARBITRARY FUNCTION FITTERS.** Models SPFX-P/N are ten-segment function fitters having uniformly-spaced fixed breakpoint voltages and adjustable slopes. SPFX-P has breakpoints for positive-going inputs and SPFX-N has breakpoints for negative-going inputs. Circuit (a) generates a function having inputs and adjustable slopes of either sign, and an adjustable origin. If all these degrees of freedom are not required, the circuit can be simplified; e.g., if the desired function has no slope change for one sign of input (b), one SPFX can be omitted. If the origin is at zero, (c), the initial offset adjustment is unnecessary. If the desired function has zero slope for zero

$$-e = \sqrt{10e_{in}} \quad \text{for } R = 20 \text{ k}\Omega \quad (2-46)$$

If an exponential network, such as Model SPLOG\*, is used, the response becomes: ( $e_2 < 0$ )

$$e = \log_{10} \left( -\frac{e_2}{0.1 \text{ V}} \right) \quad \text{for SPLOG-P} \quad (2-47)$$

\*SPLOG-P/N are designed to operate over a current range of four decades (.05 to .500  $\mu\text{A}$ ) with

an error (@ 25°C) of:  $\left| \frac{\delta i}{i_{\text{desired}}} \right| < .01$  for  $i > 5 \mu\text{A}$

and  $\left| \frac{\delta i}{i_{\text{max}}} \right| < .0001$  for  $i < 5 \mu\text{A}$  where

$$\delta i = |i_{\text{actual}} - i_{\text{desired}}|$$

connected to the other input terminal, in order to produce the desired squared output for either input polarity. (Absolute value computation is inherent in PSQ if both input polarities are supplied.) For positive output polarity, use PSQ-N, restricting the circuit then to negative input signals. II.42 shows a pair of Absolute Value circuits, either of which will convert  $e_1$  to a single polarity, regardless of its initial intentions, and such a circuit may be used to drive either of the input terminals shown here.

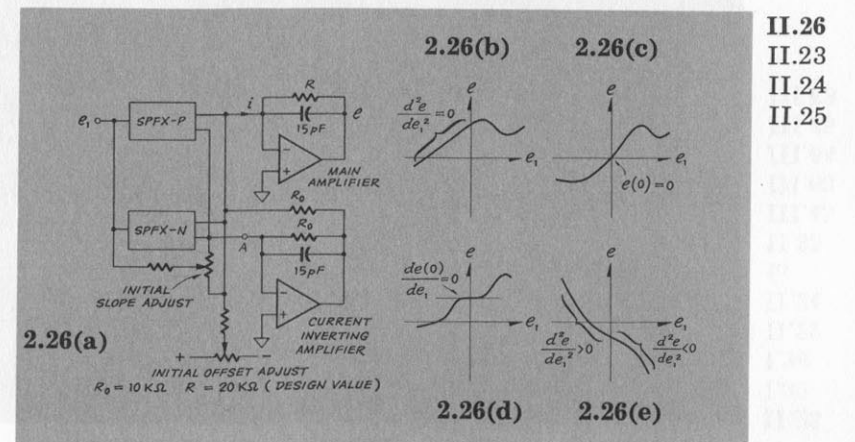
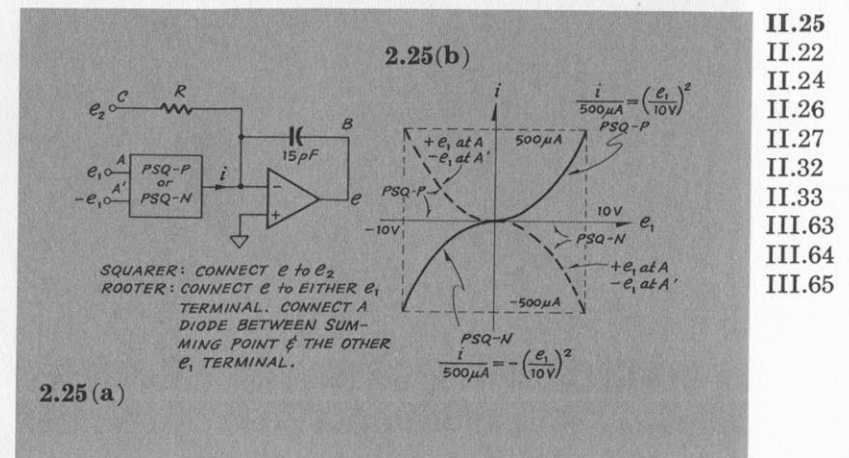
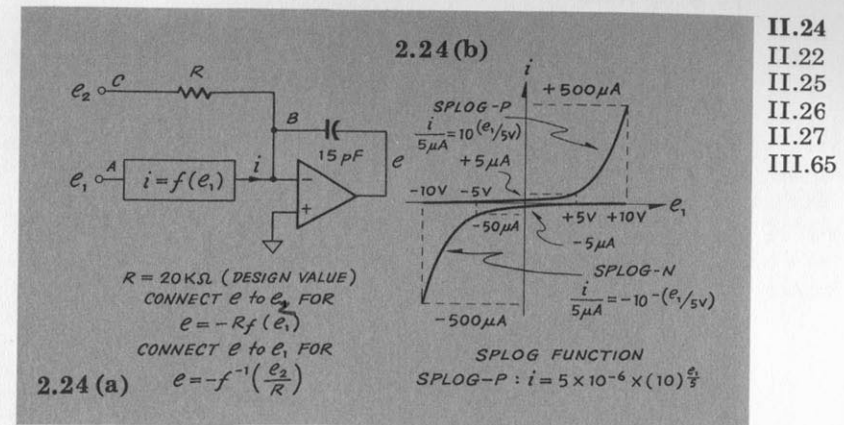
\*PSQ-P/N are designed to operate over a current range of 0 to 500  $\mu\text{A}$  with an accuracy (@ 25°C) of:  $\left| \frac{\delta i}{i_{\text{max}}} \right| < .001$  where  $\delta i = i_{\text{actual}} - i_{\text{desired}}$ .

input (d), the initial slope adjustment is unnecessary. Finally, if the desired function has monotonically decreasing slope (negative or zero second derivative) for a positive input and a monotonically increasing slope for a negative input (e) the inverting amplifier is unnecessary (ground point A).

The maximum slope change per straight line segment is 20  $\mu\text{A}/\text{volt}/\text{volt}$ .

The amplifier output may be scaled by choosing the value of the feedback resistor  $R$  so that:

$$R \left| \frac{d^2 i}{de_1^2} \right|_{\text{max}} > \left| \frac{d^2 e}{de_1^2} \right|_{\text{max desired}} \quad (2-50)$$



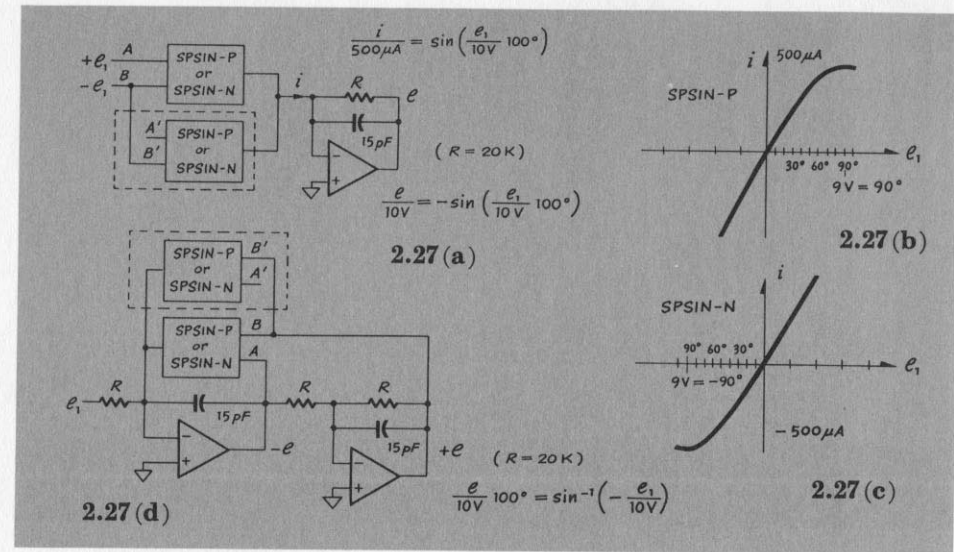


**II.27 SINE-COSINE FUNCTION FITTER (SINUSOIDAL TRANSDUCTORS).** The Philbrick SPSIN-P and SPSIN-N are diode-resistor function fitters having output currents proportional to the trigonometric sine of the input voltages.\* They require two input voltages,  $e_1$  and  $-e_1$  as shown in (a). The response of the SPSIN-P is shown in (b). Since the sine is nearly the same as the angle itself for small angles, the useful range of the SPSIN-P includes small negative voltages.

SPSIN-N behaves as shown in (c).<sup>\*</sup> By using a P and an N type together (additional unit inside dashed line of figure a) the sine function can be generated over a range of  $-100^\circ$  to  $+100^\circ$ . Note that the polarity of the output can be changed by interchanging inputs  $e_1$  and  $-e_1$ . Generation of the inverse function, arcsine, is shown in (d). In the conversion of rectangular to polar coordinate this circuit is the preferred method of generating the angular co-ordinate, for angles less than  $90^\circ$ . The dashed line indicates the additional unit necessary for outputs of either polarity. Both devices are scaled to 10 degrees per volt of input.

\*The accuracy of both SPSIN-P and SPSIN-N (@  $25^\circ\text{C}$ ) is

$$\left| \frac{\delta_i}{i_{\max}} \right| < .001 \text{ for } -1 \text{ V} \leq e_i \leq 10 \text{ V, where } \delta_i = i_{\text{actual}} - i_{\text{desired}}$$

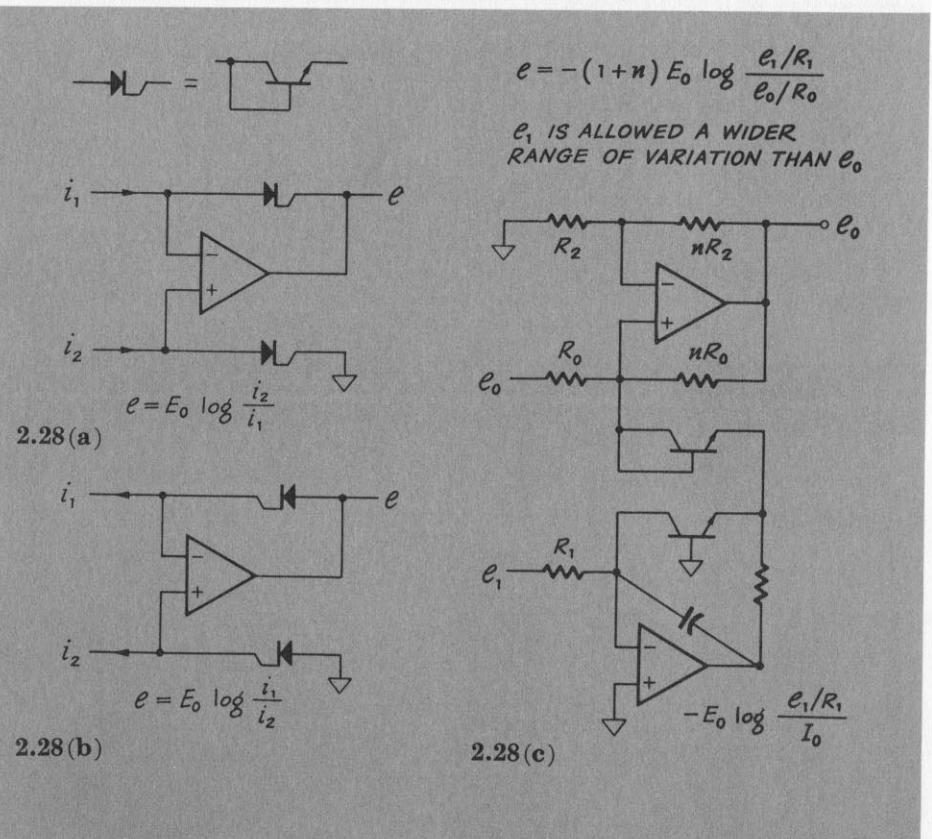


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II.28  
to  
II.33

**II.28 LOG OF RATIO CIRCUITS.** Circuits (a) and (b) show two connections in which one may incorporate a diode-connected dual logarithmic transconductor (such as the PPL-1-N/P) and, with the aid of a differential amplifier, create an output voltage that is proportional to the logarithm of the ratio of the two input currents (note that an input voltage may not be directly converted to an input current, since the amplifier input terminals are not at ground potential). The  $\log$  of voltage ratio will be seen later in this section. It is obvious that these circuits, although perfectly straightforward as they are drawn, have the limitation that they will operate only with unidirectional currents. It is possible to compute the logarithm of the ratio of input currents going in opposite directions (log of negative ratio), and it is also possible to parallel logarithmic units with those of reverse, or complementary, polarity, but please note that reversing the input polarities inverts the ratio, which is sometimes unfortunate (particularly if unsuspected).

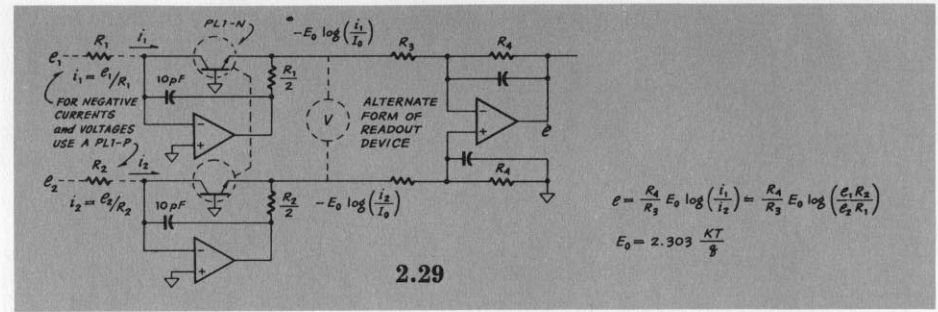
Circuit (c) shows how to obtain the log of the ratio of two input voltages. The lower amplifier, recognizable from the discussion of II.22, computes the logarithm of the numerator (about 59 mV per decade at room temperature), and the upper amplifier functions as a current pump in the Howland Circuit (see III.6), that injects a current proportional to the denominator. The difference between the diode voltages (the log of the ratio) appears at the positive input of the Howland circuit, and is magnified by the gain ratio  $(1 + n)$ .

If the ratio is to a fixed quantity, one single-ended amplifier may be used with the Philbrick PPL4 P/N (or SPL4 P/N) to obtain a wideband compensated logarithm useful over 5 decades, having both slope (nominally one volt per decade) and reference current adjustable.



II.28  
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II.29  
to  
II.33

**II.29 LOG OF LOW-CURRENT RATIO.** This circuit is recommended for obtaining the log of the current ratio at low currents. It employs transistors in the transdiode connection, which provide at least two decades more current range than can be obtained from diode-connection of the same transistors. The subtractor that follows the two identical log-function circuits then computes the log of the ratio (the difference of the logarithms). Inputs that are current sources (such as photomultiplier tubes) tolerate larger amplifier input voltage offsets than do voltage sources. The SP2A amplifier is suitable for high-impedance (current) sources, and the SP656 for voltage sources. The output amplifier requires good common-mode rejection. Temperature variation of  $E_0$  can be compensated by appropriate temperature coefficients for  $R_3$ .



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to  
II.28  
II.30  
to  
II.33

**II.30 LOG MULTIPLIER CIRCUIT.** This circuit produces an output of:

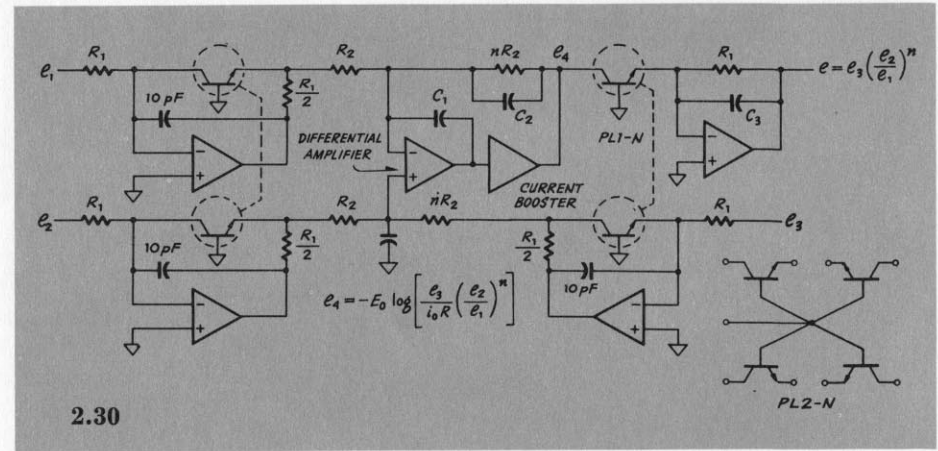
$$e = e_3 \left( \frac{e_2}{e_1} \right)^n \quad (2-53)$$

precisely over many decades, by taking the anti-log of the signal at point A which, for positive values of  $e_1$ ,  $e_2$ , and  $e_3$ , is negative and of the form:

$$-E_0 \log \left[ \frac{e_3/R}{I_0} \left( \frac{e_2}{e_1} \right)^n \right] \quad (2-54)$$

This signal is produced by feeding, to the subtractor circuit in the center of the diagram, the following inputs: (1) the log of  $e_1$ , for which it has the gain  $(-n)$ ; (2) the log of  $e_2$ , for which it has the gain  $(+n)$ ; (3) the log of  $e_3$ , for which it has unity-gain. Note that this is essentially a one-quadrant circuit.

The exponent,  $n$ , is determined by the gain of the difference amplifier, which can be adjusted by changing a single resistor in a differential TEE network, (III.81) in the input circuit ( $n < 1$ ) or feedback circuit ( $n > 1$ ).



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III.68

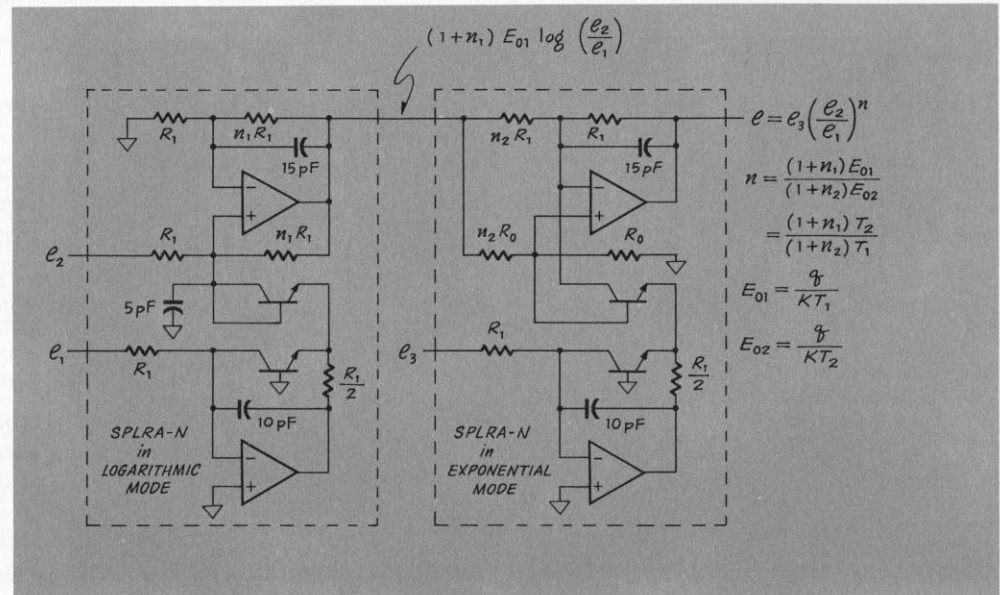
**II.31 LOG MULTIPLIER (USING LOG RATIO CIRCUITS).** The Philbrick Log Ratio Amplifiers (SPLRA-P or N) and Log Ratio Transconductors (SPLR-P or N) make convenient "building blocks" for a logarithmic multiplier. The circuit shows two SPLRA-N Log Ratio amplifiers connected to give an output

$$e = e_3 \left( \frac{e_2}{e_1} \right)^n \quad \text{where} \quad n = \frac{(1+n_1)E_{01}}{(1+n_2)E_{02}} = \frac{(1+n_1)T_2}{(1+n_2)T_1} \quad (2-55)$$

The transconductor version is the same, except that the lower amplifier in each unit must be provided separately. The gains of the two units,  $(1+n_1)$  and  $(1+n_2)$  are used to compensate for any slight differences in the junction temperatures ( $T_1$ ,  $T_2$ ) of the two units, or alternately can be adjusted to give  $n$  any value between approximately 1/5 and 5. Transistor mismatch error appears as a constant scaling error in one or more of the inputs and can be removed by changing the gain of the affected inputs (small adjustable resistors in series with each input is the simplest method). When these adjustments are made accuracies of the order of

$$\left| \frac{\delta e}{e_{\text{desired}}} \right| \ll .001 \quad \delta e = e_{\text{actual}} - e_{\text{desired}} \quad (2.56)$$

can be obtained over three decades of input voltages. The circuit shown works for positive input voltages. Use SPLRA-P for negative inputs.



II.31  
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III.64  
III.65  
III.68



**II.32 QUARTER-SQUARE MULTIPLIER.** All of the circuitry to the left of the dashed line is devoted to adding, subtracting, and weighting  $e_1$  and  $e_2$  (by what should be, at this point, thoroughly familiar techniques) to produce the four signals that are fed into the PSQ-N and PSQ-P squaring circuits, the outputs of which are fed to the inverting adder that completes the circuit. The few lines of algebra that follow prove that the output will, indeed, be proportional to the product of  $e_1$  and  $e_2$ .

$$\begin{aligned} i_a &= -(.5 \text{ mA}) \left( \frac{e_1 + e_2}{20 \text{ V}} \right)^2 \\ i_b &= (.5 \text{ mA}) \left( \frac{e_1 - e_2}{20 \text{ V}} \right)^2 \\ -e &= (20 \text{ k}\Omega) (i_a + i_b) \\ e &= (10 \text{ V}) \left[ \left( \frac{e_1 - e_2}{20 \text{ V}} \right)^2 - \left( \frac{e_1 + e_2}{20 \text{ V}} \right)^2 \right] = \frac{e_1 e_2}{10 \text{ V}} \end{aligned} \quad (2-57)$$

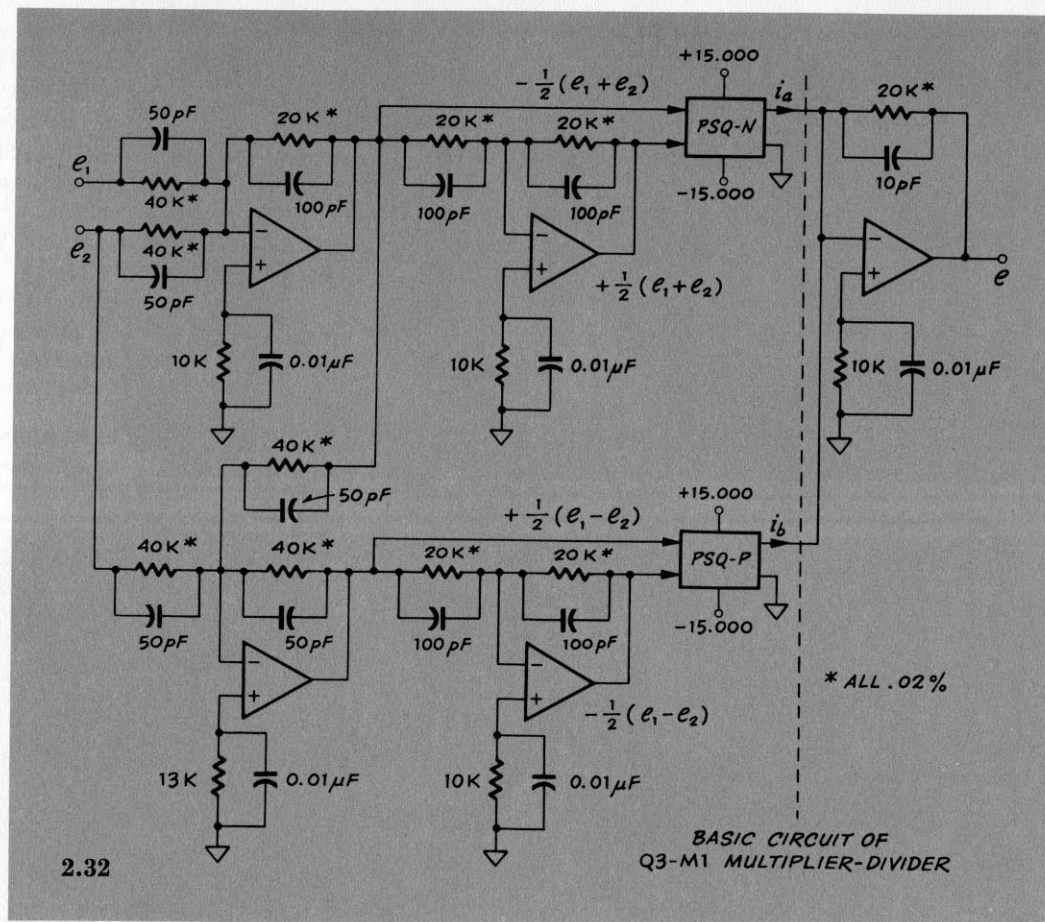
Note that this circuit is a true *four-quadrant* multiplier, capable of producing an output of either polarity, as demanded by any arbitrary combination of the polarities of  $e_1$  and  $e_2$ .

When high-speed amplifiers are used (such as the P65AH) the frequency response of the multiplier is limited by the squaring circuits, the time constant of which is approximately  $0.3 \mu\text{sec}$ .

By interchanging the PSQ-P and PSQ-N the output polarity is changed, giving

$$e = -\frac{e_1 e_2}{10 \text{ V}} \quad (2-58)$$

This circuit may also be used to accomplish division, and the next Section is devoted to that subject.



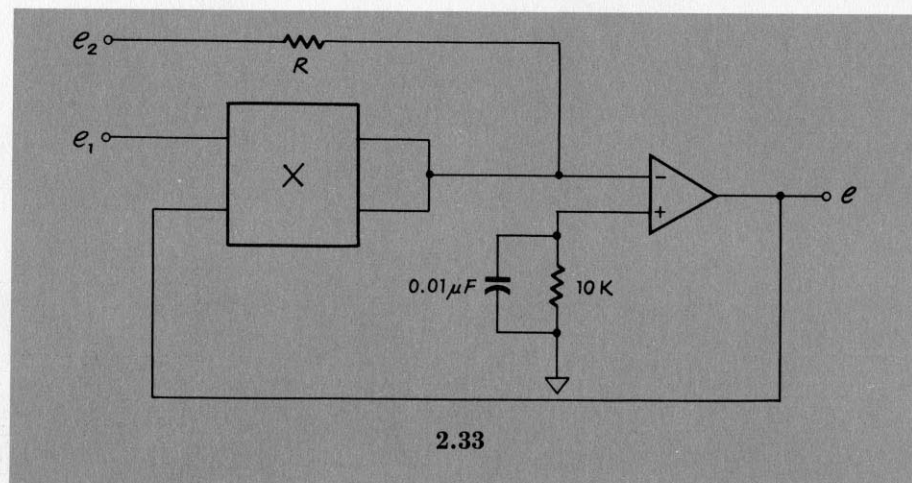
2.32

II.32  
II.22  
to  
II.31  
II.33  
III.45  
III.63  
III.64  
III.65  
III.68

**II.33 QUARTER-SQUARE DIVIDER.** If we represent all of the circuitry to the left of the dashed line in figure 2.32 by a rectangle marked "X," then the circuit shown here is an effective divider; that is:

$$e = \left( \frac{20 \text{ k}\Omega}{R} \right) \left( 10 \text{ V} \frac{e_2}{e_1} \right) \quad (2-59)$$

There is very little difference between this circuit and that of the multiplier of II.32, except that the output of the final summing amplifier is connected back to one of the old multiplier inputs, and the other input ( $e_2$ ) is fed directly into the summing point through a resistor of appropriate value for correct weighting. One degree of freedom has been lost, however: the polarity of  $e_1$  must now be negative. (If the output polarity has been changed by interchanging the PSQ-P and PSQ-N then  $e_1$  must be positive.) In all other respects, the accuracy and range of the multiplier circuit of II.32 are preserved. Output errors increase in inverse proportion to  $e_1$ .



2.33

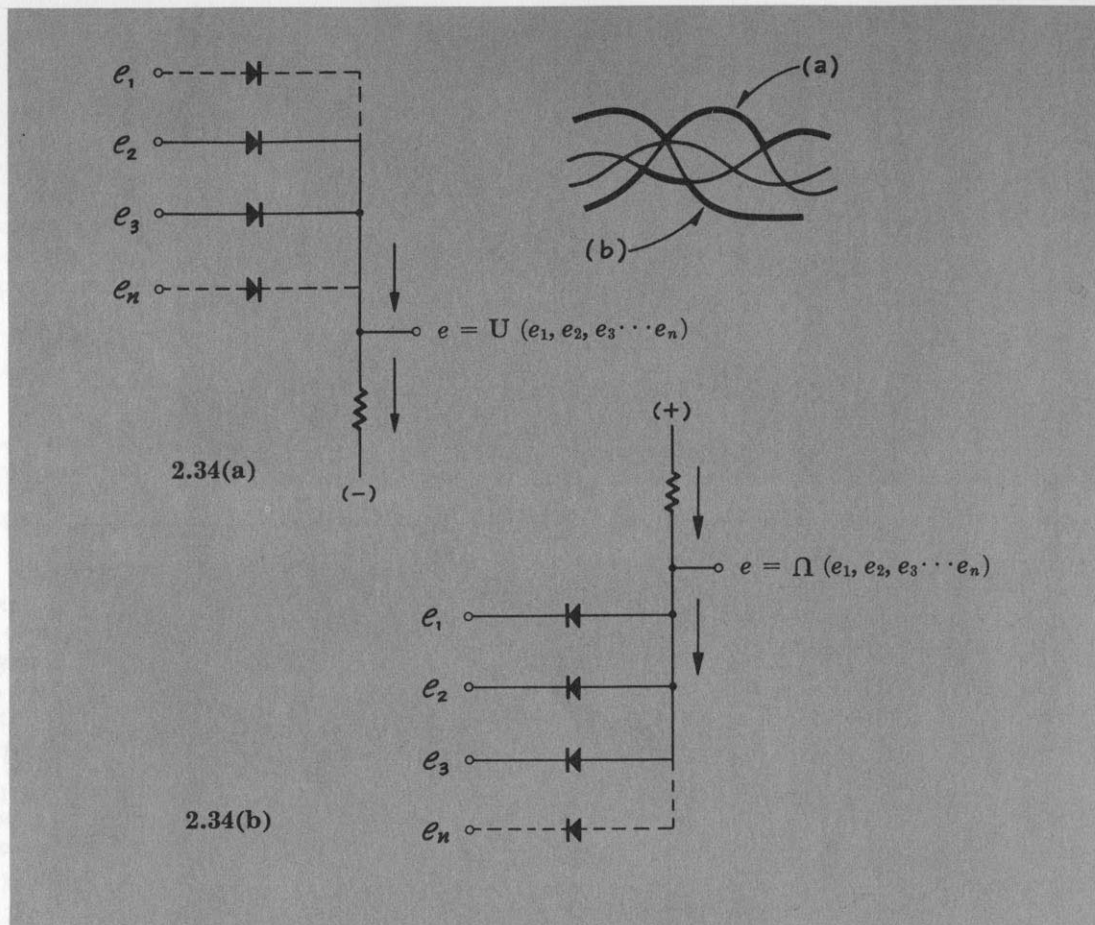
II.33  
II.22  
to  
II.32

**II.34 ELEMENTARY SELECTOR CIRCUITS.** In circuit (a), the output voltage will always be at a potential equal to the highest of the input voltages, minus the diode drop. Thus, (except at near equality) only one diode can conduct at any instant, and at least one *must* conduct, assuming that the negative supply is lower in potential than any of the inputs may ever be. The resistor is proportioned to provide sufficient current to maintain adequate speed at the lowest voltage, yet limit the diode current to a specified maximum value for the *highest* voltage anticipated. For fast switching circuits, it is best to design for as much diode current as can comfortably be allotted to the Selector Circuit, so that stray capacitance effects are minimized.

The output of circuit (b) is always equal to the lowest input voltage, *plus* the diode drop. Once again, we assume that no input voltage can be higher than the positive supply, and we advocate designing for the highest comfortable diode current.

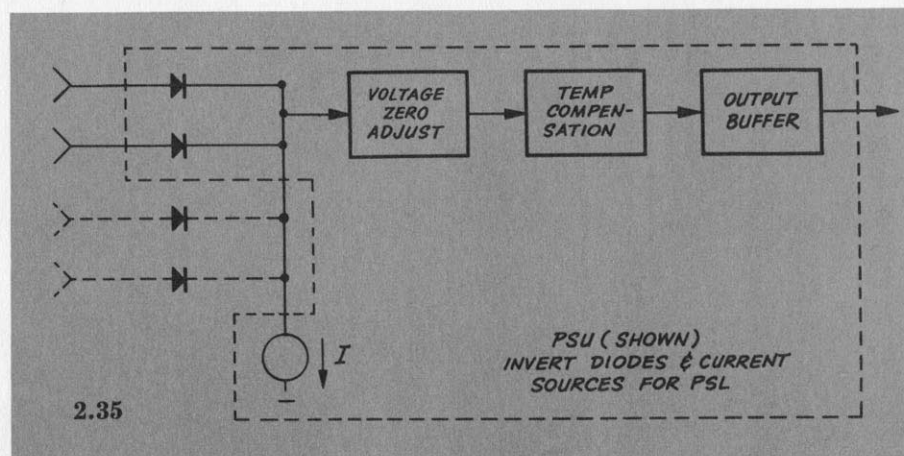
To achieve compensation that is independent of signal amplitude, even when the largest signal is very close to the return supply in magnitude, we recommend constant-current sources instead of resistors—see III.9.

The Upper Selector can be thought of as presenting at its output the most positive (or least negative) of its input voltages. As shown in 2.34(b) it presents to its output the “upper envelope” of all the input signals. Similarly, the lower selector presents to its output the most negative (or least positive) of its inputs, i.e., the “lower envelope” of all the input signals.



**II.35 COMPENSATED SELECTOR.** Although Selection is simple enough in concept, Selector circuits require certain refinements if their performance is to approach the ideal described in II.34.

These features are incorporated in Philbrick standard Upper and Lower Selectors, designated the PSU and PSL respectively. As shown here, a constant-current source (*I*) draws current from one or the other of a pair of diodes. The diodes are carefully matched at the current level established by the source. (If Selection among more than two voltage variables is required, the user may connect additional diodes of a recommended type to the selection node.) A voltage adjustment is included in the PSU/PSL design, enabling the user to establish zero output for zero input. This is done by grounding one input, leaving the other(s) open, and adjusting for zero output. The temperature compensation provided in the PSU/PSL design achieves thermometric insensitivity comparable to that of wirewound resistors. Finally, an output buffer amplifier aids error-free cascading of Selectors and provides adequate output-current capability for driving computer amplifier inputs.



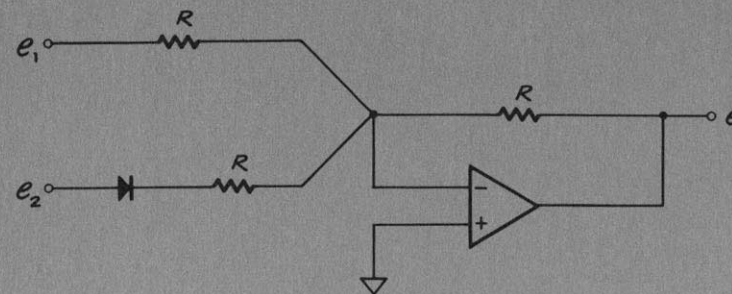
II.34  
I.32  
II.35  
to  
II.44  
III.8  
III.58  
III.74  
III.79  
III.81

II.35  
I.32  
II.34  
II.36  
to  
II.44  
III.8  
III.58  
III.74  
III.79  
III.81



**II.36 SIMPLE DUAL-MODE CIRCUIT.** The only difference between this circuit and the inverting adder of II.3 is the diode in series with  $e_2$ . The basic rules must still be followed, of course, so that the sum of the input currents must equal the feedback current, and the summing point must be very close to ground—removed only by the residual null voltage. If both inputs are positive, the output is simply the negative of the sum of the two (ignoring the diode drop). On the other hand, if  $e_2$  is negative, or if both are negative, the output is simply equal to the negative of  $e_1$ . This circuit, therefore, has two modes of operation, the choice of which depends upon the polarity of  $e_2$  with respect to ground—with  $e_2 > 0$ , the circuit is an inverting adder; and, with  $e_2 < 0$ , it is merely a unity-gain inverter with respect to  $e_1$  only.

In particular, if  $e_2$  and  $e_1$  are identical, the gain will be different for positive or negative input. Accuracy can be improved through use of a Selector circuit (see II.34, II.35), to reduce or eliminate the effect of diode drop.



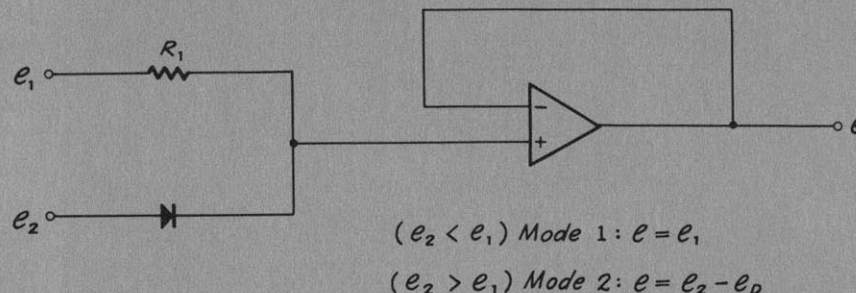
2.36

II.36  
II.34  
II.35  
II.37  
to  
II.44  
III.50  
III.63  
III.74  
III.75  
III.81

### II.37 SIMPLE DUAL MODE CIRCUIT (Non-Inverting).

This circuit will be recognized as a simple follower having two inputs. If  $e_2$  is more positive than  $e_1$ , the output is equal to  $e_2$ , ignoring the diode voltage drop.

When  $e_2$  is negative with respect to  $e_1$ , the output is equal to  $e_1$ , and the specific value of  $e_2$  has no effect on the output, provided that it is sufficiently negative to render the diode leakage current negligible. (The path for this leakage current, by the way is mostly through  $R_1$ .) The accuracy and speed can both be improved by use of a Selector circuit.



2.37

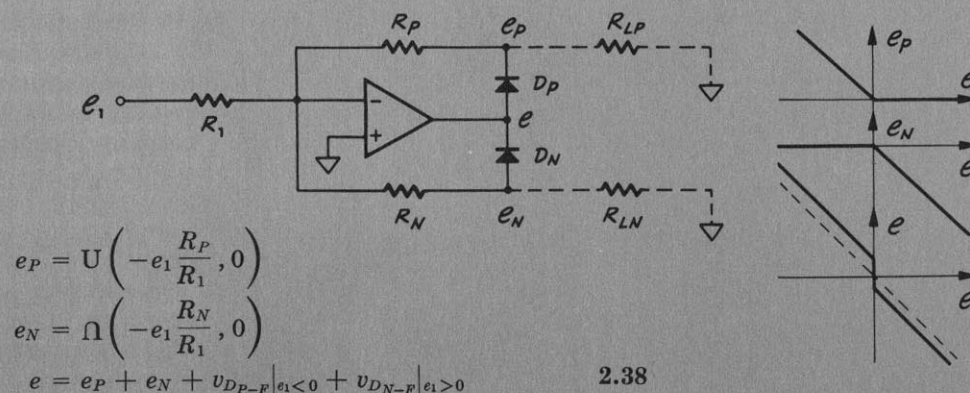
II.37  
II.34  
II.35  
II.37  
to  
II.44  
III.50  
III.63  
III.74  
III.75  
III.81

**II.38 SIGNAL POLARITY SEPARATOR.** This circuit is important for low voltage applications because it provides precisely-scaled selection of the input,  $e_1$ , with respect to ground potential, at the outputs  $e_P$  and  $e_N$ .

When  $D_P$  is not conducting,  $e_P$  is nearly zero, assuming resistive loads returned to ground (or to the virtual ground of a single-ended amplifier). The departure of  $e_P$  from zero will depend upon the reverse current of diode  $D_P$  through  $R_P$  in parallel with  $R_{LP}$ . This error can be made small and virtually constant by making  $R_N$  zero.

When  $D_P$  is conducting, the error at  $e_P$  is the forward voltage across  $D_P$  divided by the amplifier gain. Hence, precise selection may be accomplished, even when  $e_1$  is in the millivolt range.

As an added feature at the selection point ( $e_1 = 0$ ) the output  $e$  undergoes a sharp transition which may be differentiated and used as a logic signal for commanding gates or relays.



2.38

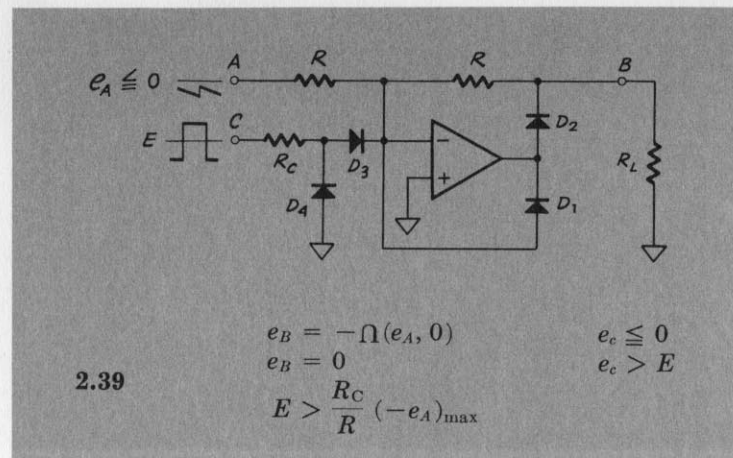
II.38  
I.25  
I.32  
II.34  
to  
II.37  
II.39  
to  
II.44

**II.39 PRECISION GATE.** When this gate is “closed” it functions as a normal unity-gain inverter between terminals A & B, for *negative* input signals. Positive input signals result in no output, because they would tend to swing the amplifier output terminal negative, which is prevented by the cooperative bounding action of  $D_1$  and  $D_2$ . When the gate is “open,” terminal A is isolated from terminal B.

The gate is swung open and shut by application of a signal to terminal C. Assuming that the resistor ( $R_C$ ) in series with terminal C is small compared to  $R$ , a positive signal of any appreciable magnitude applied to C will cause the circuit to clamp in the condition in which  $D_1$  bounds it, and  $D_2$  disconnects the amplifier

from terminal B. If terminal C is open-circuited, or returned to ground, or if a negative signal is applied to terminal C, the gate is closed, and the A-to-B circuit acts like a normal unity gain inverter... but as mentioned above, only for negative input signals applied to A. Positive input signals applied to A will open the gate, just as if they had been applied to terminal C. Note that the “closed resistance” of this switch approaches zero, to the extent that the inverter performance approaches the ideal. When the switch is open, the isolation is nearly as perfect, being somewhat dependent upon the leakage in  $D_2$ .

As in II.38, loads must be resistive and grounded.



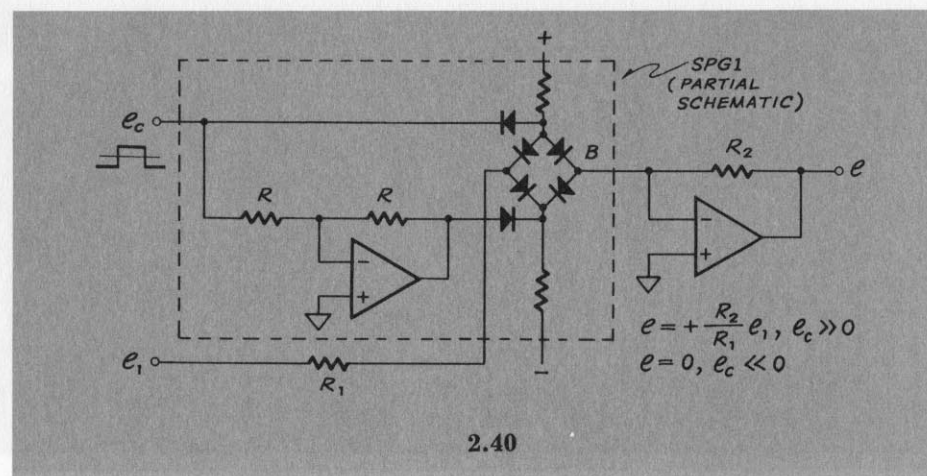
2.39

**II.40 ELECTRONIC SWITCH.** In this circuit,  $e_1$  is gated to point B when, and only when  $e_c \geq 1$  volt. The unity-gain inverter produces  $-e_c$  at the lower end of the diode bridge when  $+e_c$  is applied as shown; and, provided the magnitude of  $e_c$  is of the order of 2 volts or more, the bridge becomes conducting from  $e_1$  to B. Negative values of  $e_c$  ( $e_c \leq -1$  V) render the bridge non-conducting.

An application to which this circuit is ideally suited, and often applied, is the resetting or clamping of integrators. In such applications the corner of the bridge nearest “ $e_1$ ” is connected to the output of the integrator, and the opposite corner is connected (as shown in our diagram) to the summing point.

The reader who prides himself on commercial awareness will not be at all surprised to learn that Philbrick makes available a module, called the SPG1, in which not one, but *two* of these splendid circuits, are economically presented, in a neat and painless package.\*

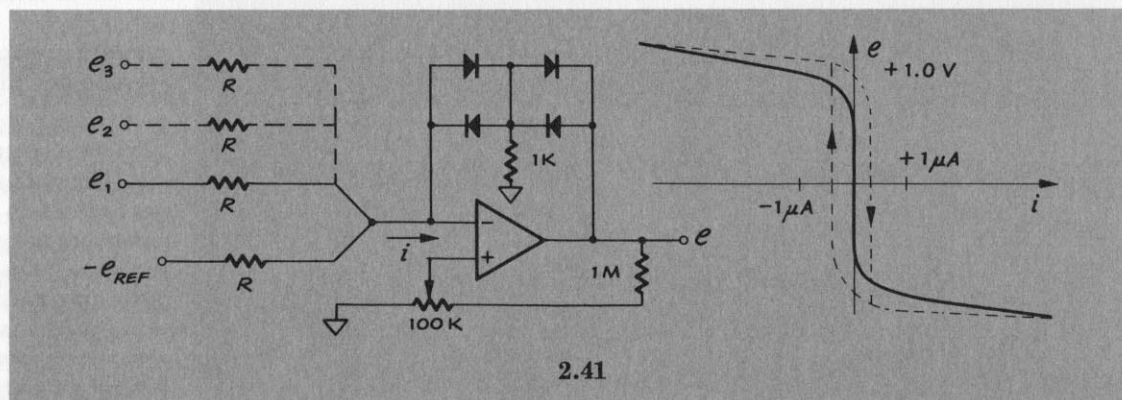
\*The SPG1 contains two complete diode bridges, and a driver stage; a single logic signal “inhibits” one bridge, “enables” the other, or vice versa, according to the signal polarity. The two bridges may be used, for example, instead of the relay circuit of II.50, for setting arbitrary initial conditions.



2.40

**II.41 PRECISION COMPARATOR.** This circuit indicates whether a voltage is greater than or less than a desired reference voltage. It does so by sensing the direction of the current,  $i$ , flowing between the input network and the amplifier summing point, and bounding the output accordingly. Since the circuit is current-sensitive, it can just as easily compare the sum of several voltages against a reference, or for that matter, against the sum of several references. Note that the reference voltage, although it need not be constant, does need to be inverted before being presented to the comparator. The output is approximately logarithmic, providing a graded null.

For very *slowly* changing voltages, “snap action” can be added by means of positive feedback, at the small price of introducing a finite amount of hysteresis. The amount of hysteresis is controlled by the potentiometer connected to the positive input (which should be grounded if snap action is not required).



2.41

II.39  
I.25  
I.32  
II.34  
to  
II.38  
II.40  
to  
II.44  
III.50  
III.58  
III.74  
III.75  
III.79  
III.81

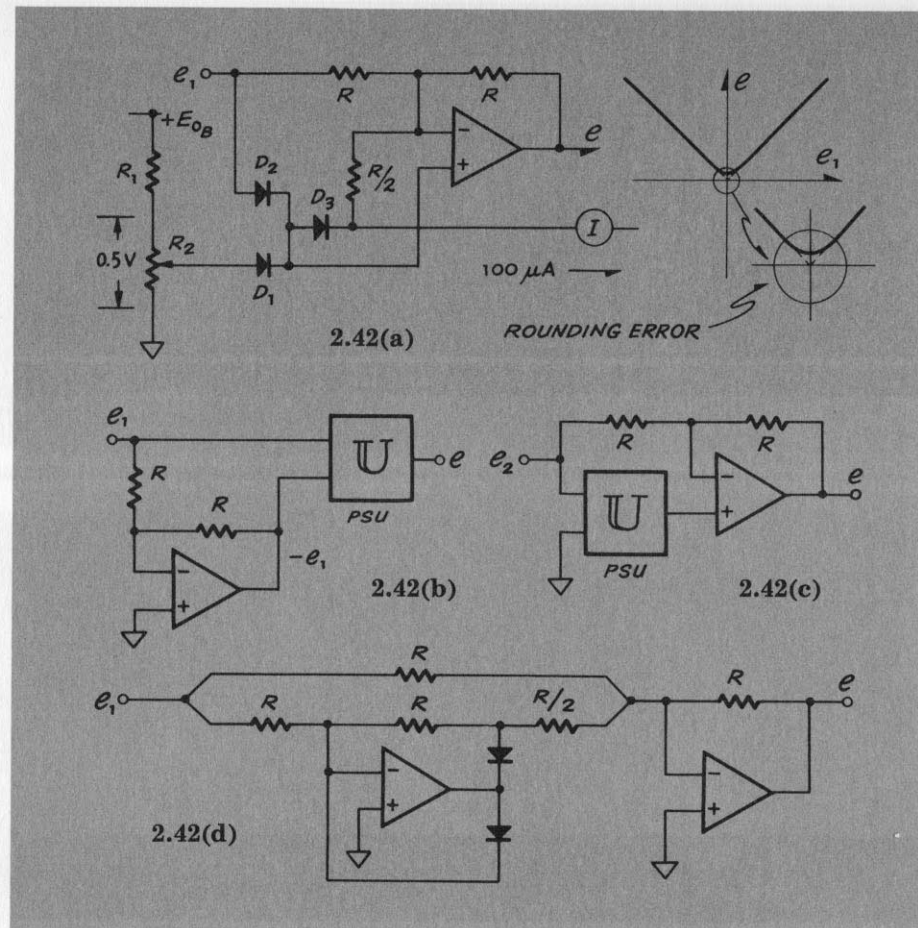
II.40  
I.25  
I.32  
II.34  
to  
II.44  
III.50  
III.58  
III.74  
III.75  
III.79  
III.81

II.41  
I.25  
I.27  
I.32  
II.34  
to  
II.44  
III.39  
III.40  
III.43  
III.44  
III.45  
III.58



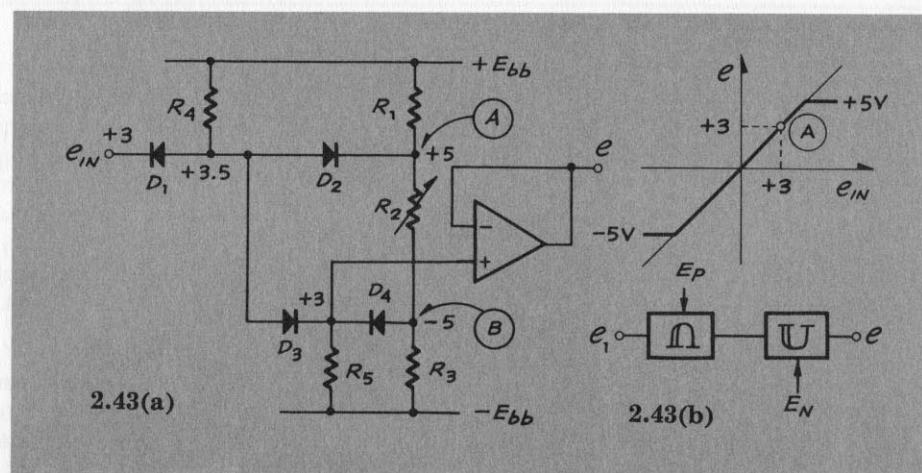
**II.42 SIMPLE ABSOLUTE-VALUE, PRECISION ABSOLUTE-VALUE CIRCUIT.** With negative input, the positive terminal of the amplifier in (a) is as close to ground potential as one can adjust the low-resistance potentiometer. Hence, negative-polarity signals find their way from  $e_1$  to  $e$  through a unity-gain inverter. Positive-going signals have three paths. One is via the unity-gain inverter. Another is via the drop of  $D_2$  to the positive input, whence a gain of (+4) is realized for  $(e_1 - V_{D2})$ . The third is via  $D_2$  and  $D_3$  in series with  $R/2$ , whence a gain of (-2) is obtained for  $(e_1 - V_{D2} - V_{D3})$ . The sum of these terms is simply  $e_1$ , if  $V_{D2} = V_{D3}$  at the suggested current. The output is, thus, a positive-going signal, equal in magnitude to the input, but of positive polarity, regardless of the input polarity. (If, for example,  $e_1$  were to be a sine wave,  $e$  would be the positive full-wave-rectified version of it.) If all diode and supply polarities were reversed, one would obtain the negative absolute value. The Philbrick PSU Upper Selector is used to obtain the absolute value in 2.42(b) and 2.42(c). In the PSU, a zero adjustment, for diode-difference compensation, is incorporated within the unit. In (b), the Selector is presented with the input voltage and its negative, and presents the greater of them at the output. A (single-ended) amplifier is required to invert the input, if its negative is not already available in the system. In (c), the PSU selects accurately between the input and ground, presenting the greater of them to the positive input. When the input is negative, inverter action takes place, because the positive input is at ground potential; when the input is positive, follower action occurs. A good differential amplifier is needed in (c), but all the advantages of a feedback amplifier are gained, including the possibility of inserting a booster in the loop for high current capability.

By placing the diodes within the feedback loop, the circuit of 2.42(d) renders them effectively "ideal." When  $e_1$  goes negative, the output of the first amplifier jumps positive by one diode drop, shutting off the upper diode and bounding the amplifier through the (conducting) lower diode. The second amplifier simply inverts the (negative)  $e_1$ . When  $e_1$  is positive, both amplifiers invert and the output is:  $e = 2e_1 - e_1 = +e_1$ , by virtue of the gain of 2 in the lower branch.



**II.43 CLIPPER.** This circuit has, in the Ideal Case, linear and unity-gain response between two sharply-defined limits, above and below which its output is constant at the limit value; thus it behaves as a "clipper," without saturation of the amplifier or other undesirable side effects. The curve illustrates its Ideal behavior for symmetrical limits of  $\pm 5$  V.  $R_2$  adjusts both limits simultaneously.

For convenience in analyzing circuit performance, we have annotated the schematic with typical voltage values, representing the prevailing conditions for a +3 V input (point A on the curve). Under these conditions,  $D_1$  and  $D_3$  are conducting, and  $D_2$  and  $D_4$  are not. Above  $e_{in} = 5$  V,  $D_2$  conducts, clamping the output at +5 V. Below  $e_{in} = -5$  V,  $D_4$  conducts, clamping the output at -5 V. For good accuracy, the forward drop of  $D_1$  should match that of  $D_3$ ... a condition that could be encouraged by replacing  $R_4$  and  $R_5$  by constant-current sources (cf: II.35 and III.8), particularly if the signal excursion approaches  $E_{bb}$  in magnitude. When in lower bounds, diode drop in  $D_4$  is not compensated. N.B. Selector units PSL & PSU will provide bounds having accuracy, temperature and diode-difference compensation, and low output impedance—sans amplifier!



II.42  
I.25  
I.32  
II.34  
to  
II.41  
II.43  
II.44  
III.52  
III.53  
III.54  
III.63  
III.64  
III.65  
III.81

II.43  
I.25  
I.32  
II.34  
to  
II.42  
II.44  
III.8  
III.15  
III.58  
III.66  
III.67

**II.44 DEAD ZONE.** This circuit establishes a region of almost complete insensitivity to small values of input.

$$-E \frac{R_2}{R_1} < e < E \frac{R_4}{R_3} \quad (2-59)$$

In that region, both  $D_1$  and  $D_2$  are reverse-biased.  $D_3$  and  $D_4$  limit the reverse bias, and hence block both the leakage current and any stray capacitive coupling from the input terminal to the amplifier.

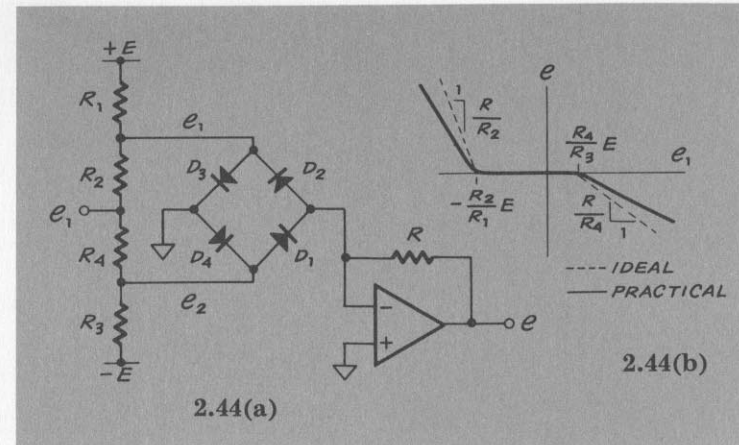
When  $e_1$  becomes sufficiently large,  $D_1$  or  $D_2$  conducts. The output voltage is approximately:

$$e = -\frac{R}{R_2} \left( e_1 + \frac{R_2}{R_1} E \right), e_1 \text{ neg.} \quad (2-60)$$

$$e = -\frac{R}{R_4} \left( e_1 - \frac{R_4}{R_3} E \right), e_1 \text{ pos.} \quad (2-61)$$

In both expressions, diode offset has been neglected. Its principal effect is to cause significant rounding at the corners of the response characteristic, as shown. Practical values for  $R_3$  and  $R_1$  may be larger than the equations would indicate.

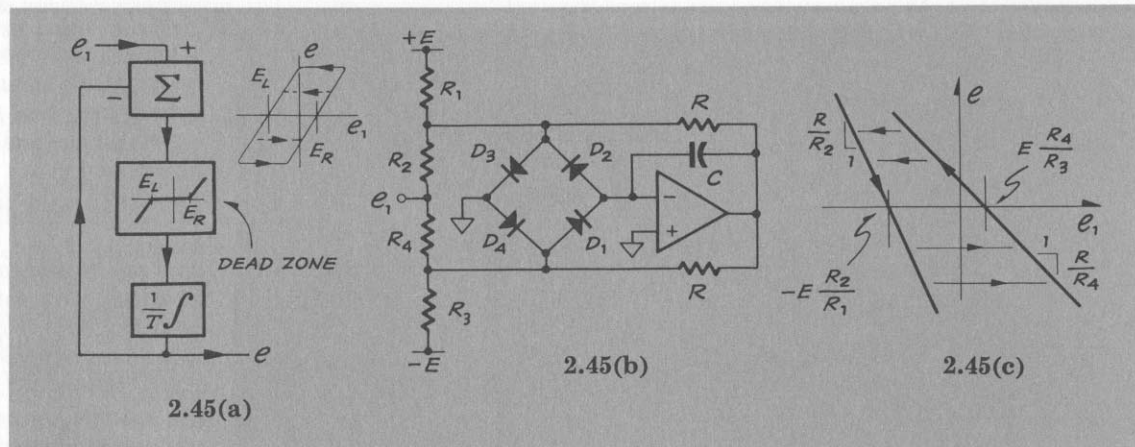
Further, these offsets are temperature-dependent (2–3 mV/°C referred to input), a source of uncertainty in the intercepts of the characteristic.  $D_1$  and  $D_2$  may each be replaced by an “ideal diode” (or polarity separator) circuit like that of II.38, virtually eliminating the effect of diode offsets. The dashed resistor—when used—permits symmetrical adjustment of the thresholds by means of a single adjustable element.



II.44  
I.32  
II.34  
to  
II.43  
III.58  
III.77  
III.79

**II.45 BACKLASH SIMULATION.** Backlash (often called hysteresis) may be simulated by applying a circuit having the dead-zone characteristic described in II.44 to a feedback loop like the one shown in (a). Circuit (b) is a practical realization of 2.44(a), providing the required summing and integrating capabilities.

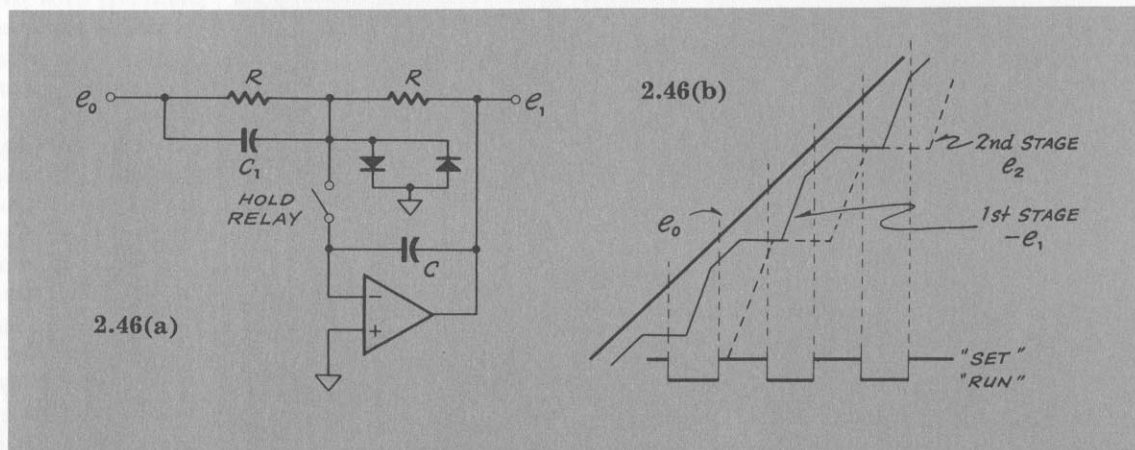
When the input is changing, and the output is beyond the transition region the output lags the input in a manner determined by the time constant  $RC$ . (To minimize this lag, minimize  $RC$ .) When the output is in the transition region (diodes  $D_1$  and  $D_2$  both reverse-biased) the output drifts at a rate equal to the net leakage current into the summing point divided by  $C$ . Hence, the diodes, the amplifier, and the capacitor should be chosen for minimum leakage. The choice of  $C$  must therefore reflect a compromise between tracking speed and holding accuracy.



II.45  
III.77

#### II.46 TRACK AND HOLD MEMORY (Relay Switching).

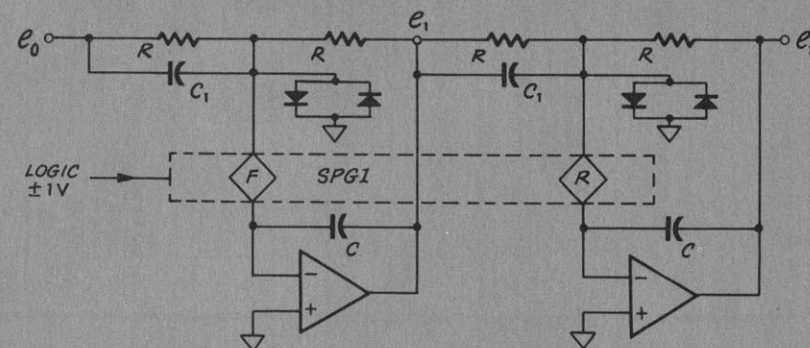
The Philbrick SPREL set-hold relay pair is an excellent way of equipping an integrator with Track-and-Hold capability, using circuit (a). Choose  $C$  to achieve the hold accuracy required (see II.10 and II.11).  $R$  must be low enough in resistance so that  $RC$  is a small enough time constant to permit accurate tracking of the fastest-changing signal expected. The capacitor  $C_1$  can be chosen so that the ratio of the feedback time constant to the input time constant is the same as the ratio of the closed-to-open switching times of the relay. The second relay in the SPREL operates in a complementary manner to the first and, can be used in a second-stage track-hold circuit, by driving the logic input appropriately. (Two stages of Track-Hold are often required so that the second can hold the previous result while the first is taking a new sample.) The ramp response typical of (a) is shown in (b).



II.46  
I.33  
I.34  
I.36  
II.47  
III.53  
III.56  
III.57  
III.74  
III.75  
III.76



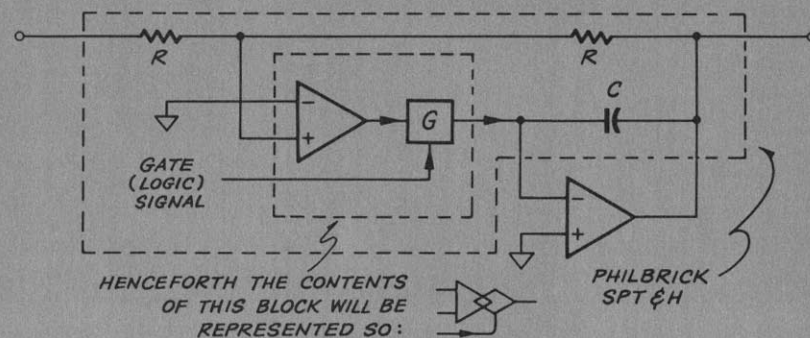
**II.47 TRACK-HOLD MEMORY (Electronic Switching).** The Philbrick SPG1 (see II.40) can be used to replace the SPREL circuit of II.46. In the circuit shown here, which embodies two stages, as suggested in II.46  $C_1$  must equal  $C$ , since the diode switch operates virtually instantaneously . . . at least in comparison with the RC time constants. The major disadvantage of this circuit is the required long recovery (sampling) time, while the output relaxes exponentially (following the RC feedback time constant) from the value it had in the previous Hold state to the value it must have in the Track state. This problem can be largely eliminated by using the circuit of II.48. Leakage in the Hold mode may be a problem, particularly at high temperatures. The Waveforms that would describe the behavior of 2.47 are similar to those in Figure 2.46(b), except that there is no relay-operating-time delay.



2.47

**II.48 TRACK-HOLD MEMORY (Gated Amplifier).** Here a gated amplifier replaces the electronic switch used in II.47, and the relay used in II.46, as the device that shifts the circuit from the Track mode to the Hold mode. Used as a current amplifier, to increase the speed of tracking by providing more charging current, it need not have voltage gain. It must be non-inverting, and, when gated off, must exhibit as little leakage as possible to the amplifier input. For stability, it must have little phase shift up to the maximum frequency for which the loop gain of the amplifier-cum-integrator is greater than unity, and must have at least as small input uncertainty as the computing amplifier, though its input leakage current is less important.

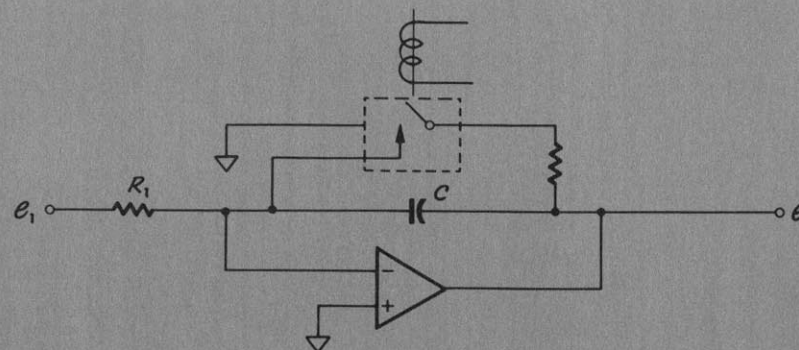
Anticipating your desire for a convenient and economical “black box” we have invented the Philbrick SPT&H, which will also perform peak—and valley—following operations, at the flick of a switch. (See III.53.)



2.48

**II.49 ZERO-VOLT RESET.** Integrators must be reset to appropriate initial conditions, before each new computing cycle begins. Here we show a relay discharging the feedback capacitor to zero, thus resetting the output to zero. A small series resistor limits the capacitor discharge current to protect the relay contact and the capacitor. This resistor should be no larger than necessary, since it can allow the circuit to reach an equilibrium significantly different from zero, if its resistance is significant with respect to  $R_1$ .

Three caveats: (1) Minimize leakage across the relay contacts, or the circuit will approach the function of a high-gain unit-lag, rather than a true integrator; (2) Poorly-chosen relay coils may induce an “inductive kick” into surrounding circuitry, unless damped. This occurs when the relay is deenergized (the worst possible time—just as integrating begins again); (3) Leakage and stray capacitance from the relay drive potential to the summing point can be far more serious than leakage across the contacts, because that voltage can be as high as the power supply. Hence, this switch should be appropriately shielded and grounded.



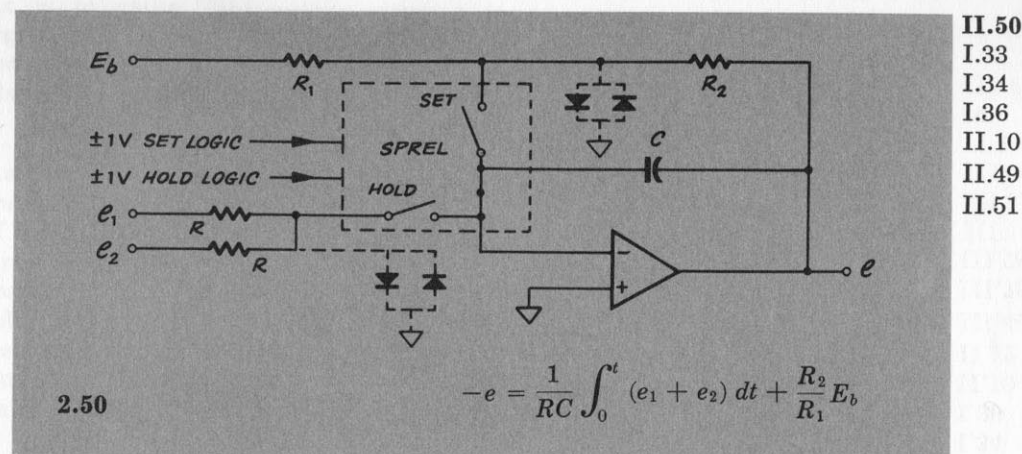
2.49

II.47  
I.33  
I.34  
II.40  
II.46  
II.48  
III.49  
III.50  
to  
III.53  
III.74  
to  
III.76

II.48  
I.33  
I.34  
II.39  
II.46  
II.47  
II.51  
III.49  
to  
III.53  
III.74  
III.75  
III.76

II.49  
I.34  
I.36  
II.10  
II.12  
III.46  
III.75  
III.76

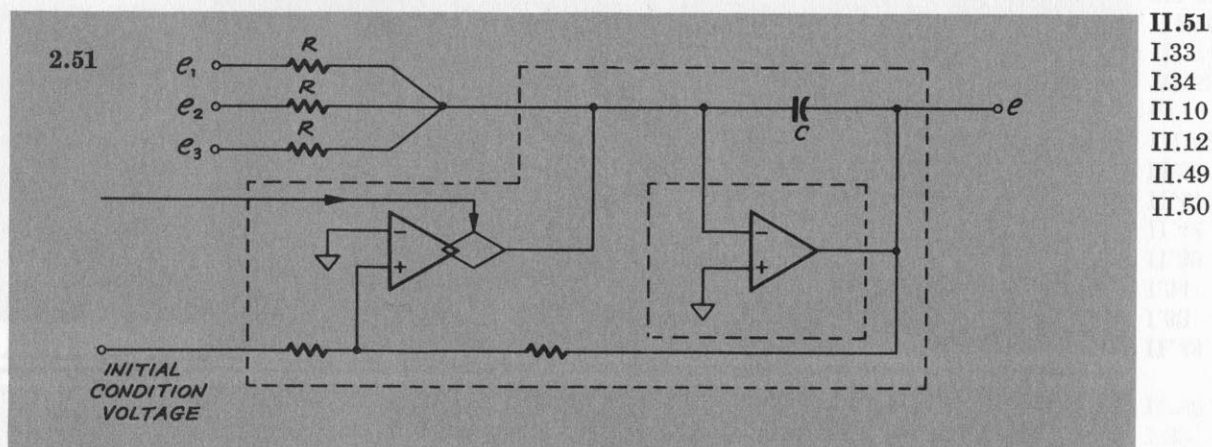
**II.50 INITIAL CONDITIONS RESET.** The Philbrick SPREL set-run reed relay pair is designed for this application. Resetting will be accomplished with the time constant  $R_2C$ ; hence,  $R_2$  must be low for fast reset. However, the  $R_1, R_2$  network must not be so low in resistance as to overload either the amplifier or the initial-condition source,  $E_b$ . Independent logic input signals may be fed to the SPREL to control the Set and Hold modes. The diode clamps shown in dashed lines will help to reduce both AC and DC leakage currents across the relay.



## II.51 INITIAL-CONDITIONS RESET (Gated Amplifier).

Here we show a gated amplifier (non-inverting), used as a means of very quickly resetting a summing integrator to an initial condition. The circuit is identical in function to that of II.50, except that the gated amplifier is inherently faster than the relay, and the integrating network is not disconnected, because the gated amplifier has established a new summing-point for the Reset condition. See II.39.

The Philbrick SPT&H may serve in this capacity as well, provided that its built-in  $0.01 \mu\text{F}$  integrating capacitor is suitable. Larger capacitors may of course be connected externally and will then be in parallel with the  $0.01 \mu\text{F}$  already inside the SPT&H.





## PART THREE INSTRUMENTATION

---

The raw materials for these applications were gathered, described, and explained in Part I. The configurations in which we have arranged those materials have all appeared and been analyzed in Part II . . . for all measurement is information conversion, and all such conversions fall into one class or another of data manipulation—computing, in its broadest sense.

This Anthology of well over 100 Circuits That Work has been culled (not without great pain) from the Augean files of our Applications Engineering and Development Engineering departments. Time and Space permitting, we might have gone on for at least another 100, without significant repetition or overlap, but our rule was to select a good example of each genus, rarely admitting more than one or two species, and almost never more than one specimen of each. Despite its imperfections, for which we apologize in advance, we believe this to be the largest and most panoramic collection of Operational Amplifier Instrumentation applications ever assembled and catalogued.

Some idea of the pace and vigor of this field may be gained from the fact that we have twice had to revise and expand this section, *in the year or so during which it was written*, to include new circuits that could not, in our judgment, be ignored.

One thought more about the nature of these circuits: only a few of them have been selected because they were—even in our opinion—the best of their kind. All are representative of good current practice, yes. In its class, each has been fashioned to enhance some one characteristic: economy, simplicity, accuracy, convenience, etc. The few that *are*, to our knowledge, very close to the limit of the current state of the Analog Art are so identified, at least by inference. As for the great majority of these circuits—use them with confidence, but do not despair if they are not adequate to the task you have set for them; instead, call on us to dip back into those files again. For every circuit you see here, we have a dozen variations in stock; one of them is almost sure to serve.

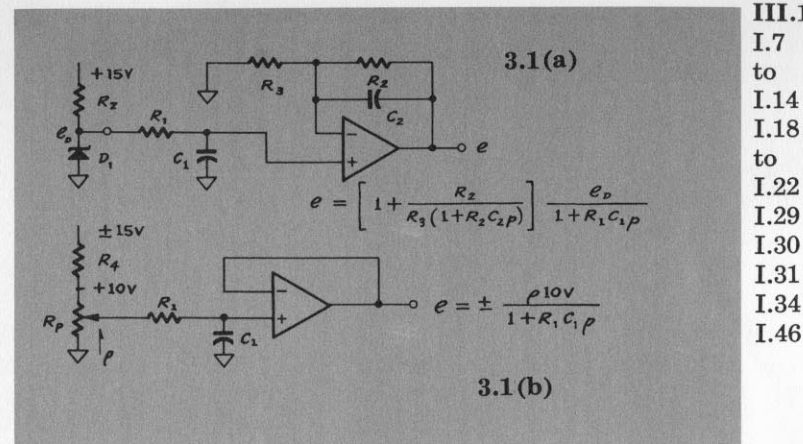
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III. 1- 9	Energy Sources . . . . .	64 - 68
III.10-21	Signal Sources . . . . .	68 - 74
III.22-28	Filters . . . . .	74 - 78
III.29-42	Signal Conditioners . . . . .	79 - 84
III.43-81	Meters and Converters . . . . .	84-102

**III.1 FIXED-VOLTAGE PRECISE REFERENCE.** In Figure (a),  $R_z$  is adjusted to set the current through the temperature-compensated zener diode to a value at which it has essentially zero temperature coefficient. Noise and pickup are attenuated by the  $R_1C_1$  filter, and the resulting voltage is amplified and buffered by a follower-with-gain circuit (see II.26). The capacitor  $C_2$  is chosen primarily not for noise reduction, but to assure dynamic stability. The gain may be trimmed to compensate for the zener tolerance and achieve the precise voltage desired at the output. The resistors  $R_1$ ,  $R_2$  and  $R_3$  should be low in value, in order

that the amplifier input offset and noise currents do not contribute significant error. However  $R_1C_1$  should be high enough for effective filtering, and  $R_2 + R_3$  should not load the amplifier output excessively.

Figure (b) provides an adjustable output voltage, using as its precise reference a stable source such as the Philbrick PR-300 (or even PR-30) power supply, or circuit (a).  $R_4$  may be trimmed so that the full-scale output (e.g., 10 V) is delivered precisely when  $\rho = 1$ . Since this circuit does not load the potentiometer, its dial calibration can be made accurate (say,  $\pm 1\%$ ) and linear.



**III.2 PRECISE VOLTAGE SOURCE.** Instead of the differential amplifier circuits described in III.1, the single-ended amplifier circuit shown here may be preferable, especially since the amplifier may then be a chopper-stabilized design. The output voltage is directly proportional to  $R_2$ , which may, for convenience, be a decade resistor box (typical range 0 to 10 k) or a (10 k) rheostat may be used. In the latter case, the input resistance,  $R_1$ , will probably have to be trimmed to accommodate the resistance tolerance of the rheostat. The dial calibration will be accurate to the limits of resolution and linearity of  $R_2$ . The RC filter shown here may require a larger value of capacitance for the same attenuation than did that of the III.1 circuits.

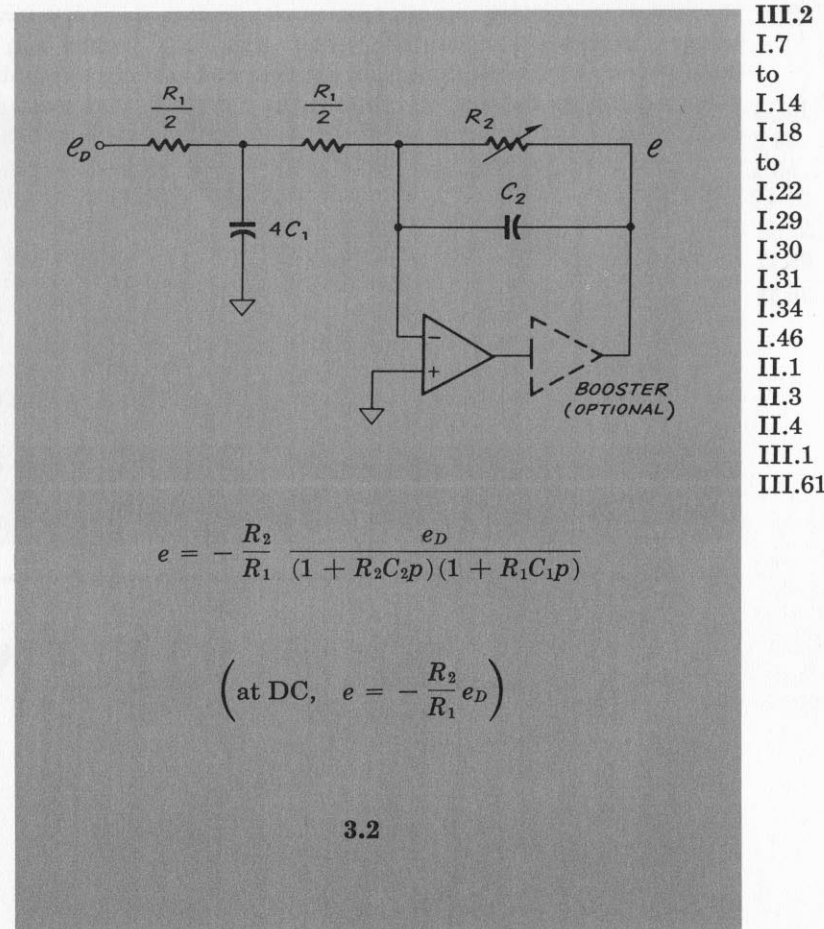
The input voltage,  $e_D$ , may be derived from a resistor and compensated zener diode circuit, as in 3.1(a). However, to achieve maximum temperature stability, that resistor,  $R_z$ , must be smaller than it was in 3.1(a), because of the input current,  $e_D/R_1$ . Alternatively,  $e_D$  may be a stable power or reference supply.

Special attention to grounding is required if the full capabilities of this circuit are to be realized. Ground returns from any heavy loads should be returned directly to the amplifier's power common at the power supply. Also, the current flowing through the zener diode (if used) should not be allowed to flow through a high-quality ground system to a remote tie point. Instead,

either tie the high-quality ground to the zener supply's power common at the zener diode, or bleed a balancing current from the negative side of the supply to the junction of the zener diode and high-quality ground. If the power supply is used as the reference, avoid corrupting the reference voltage with common-line resistive drops caused by amplifier quiescent and load currents. (This can be avoided by running separate power and reference wires between the supply and the amplifier circuit.)

The limit of error of this device may be stated as the sum of the following error sources:

- The absolute accuracy to which the input current may be established.
- The stability, against both time and temperature, of  $e_D$ .
- The absolute accuracy to which  $R_2$  is known, at the particular setting used.
- The amplifier input offset current which represents some fraction of the summing-point current, and creates a first-order error.
- The amplifier (residual) offset voltage, including drift and all other uncertainty factors (see I.14), which also constitutes a first-order error term (and is one of the factors affecting the accuracy with which the input current may be established).
- The finite-gain error factor—possibly significant for amplifiers having low gain.



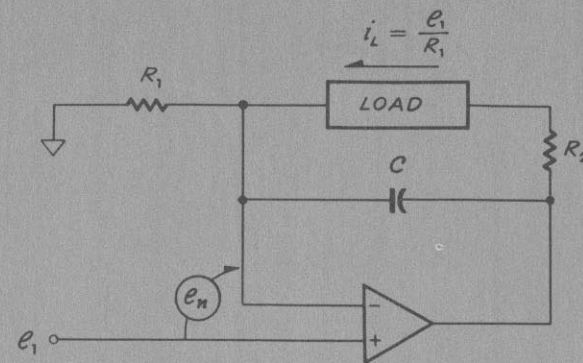


**III.3 CURRENT PUMP I—FLOATING LOAD.** This circuit is similar to the follower with gain 2.2(b) with the load replacing the feedback resistor. The amplifier is selected so that the noise and offset currents at each of its inputs cause error that is sufficiently small as to be negligible in the application. The high (low-frequency) gain of the amplifier assures that the voltage across the resistor  $R_1$  is very nearly  $e_1$ , provided that the amplifier has not saturated. The current through  $R_1$  must also flow through the load. (This current can be provided by a booster, if the amplifier cannot furnish enough.)

Special care is required to prevent the flow of heavy load current through the high-quality ground system to a remote tie point. It may be wise to put the tie point at the resistor  $R_1$ .

$R_2$  and  $C$  are selected to achieve stability. Neither is *always* required, but both are necessary when driving inductive loads. Also see 2.22(b), in which the load is a grounded-base transistor. There are innumerable active and/or non-linear loads for which this circuit may not be sufficiently stable. A more elaborate circuit will be required to drive current through such loads.

3.3



III.3  
I.7  
I.18  
I.34  
II.1  
to  
II.5  
III.4  
to  
III.9  
III.31  
III.38  
III.59  
III.80

**III.4 CURRENT PUMP II—FLOATING LOAD.** In the current pump of circuit (a) the input current is again given by  $e_1/R_1$  to the accuracy determined by the ratio of  $e_1$  to  $e_n$ . The feedback current that flows through  $R_2$  is equal to the signal input current  $i_1$ , to an accuracy determined by its ratio to the input error current of the amplifier. The voltage across  $R_3$  is  $-R_2 i_1$ , subject to the errors just described, and the booster must furnish both  $i_2$  and  $i_3 \dots$  through the load. Thus, the load current is proportional both to the input voltage and the conductance of  $R_1$ .

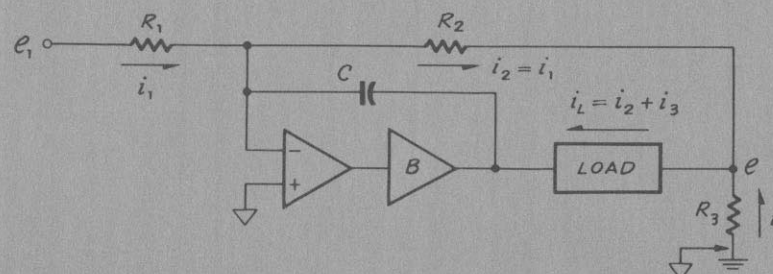
Once again, both load terminals are high, and the load may be complex and active, within the voltage and current capability of the amplifier and booster. This circuit can be used as a deflection-coil driver, in which case,  $C$  and  $R_A$  would be needed for dynamic stabilization. These components, in addition to the booster voltage-range and the deflection-coil inductance, limit the maximum rate of change of load current, which may be an important factor in deflection-system performance, particularly for a saw-tooth current wave form.

Circuit (b) shows a version of this circuit, in which the input signal,  $i_1$  is derived directly from a current source, in which case, the current pump operates simply as a current amplifier, the gain of which—i.e., the ratio of  $i_L$  to  $i_1$ —is given by:

$$\frac{i_L}{i_1} = 1 + \frac{R_2}{R_3} \quad (3-1)$$

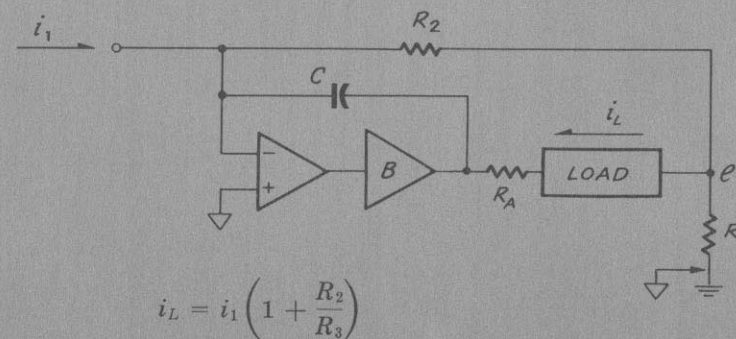
Note that the power-common symbol is used for the termination of  $R_3$ . This connection is especially recommended when the drop caused by  $i_1$  flowing through the path from high-quality ground to power common would be significant compared to  $e_1$ .

3.4(a)



$$i_L = \frac{e_1}{R_1} \left( 1 + \frac{R_2}{R_3} \right)$$

3.4(b)

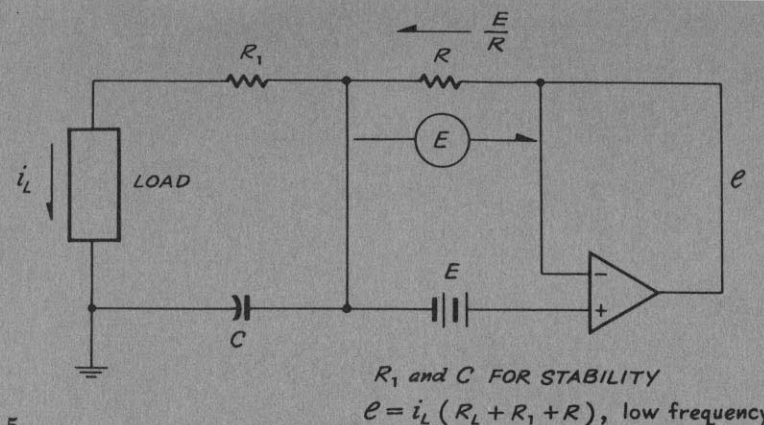


$$i_L = i_1 \left( 1 + \frac{R_2}{R_3} \right)$$

III.4  
I.7  
I.18  
I.34  
II.1  
to  
II.5  
III.3  
III.5  
to  
III.9  
III.31  
III.38  
III.59  
III.80

**III.5 CURRENT PUMP III—GROUNDED LOAD.** In this circuit, the voltage across  $R$  is equal to the reference voltage,  $E$ , within a margin of error given by the ratio  $e_n$  to  $E$ . The current through  $R$  is, therefore,  $E/R$ . Assuming that the amplifier input current is very small compared to  $E/R$ , the same current,  $E/R$ , flows through the load. Provided that the sum of  $e_L$  and  $E$  does not exceed the output voltage capability of the amplifier, and provided that  $i_L$  does not exceed its current capabilities, the circuit will drive the calculated current through any load impedance, including complex loads. Active loads can of course be driven but often tend to reduce the available voltage range, and may introduce a common-mode error factor.

This circuit has the convenience of grounding the load,  $Z_L$ , and the inconvenience of floating the reference source,  $E$ . Note that  $R$  is usually more convenient to adjust than  $E$ , to set the desired load current.  $R_1$  and  $C$  are suggested for dynamic stability, particularly if the load is reactive.



3.5

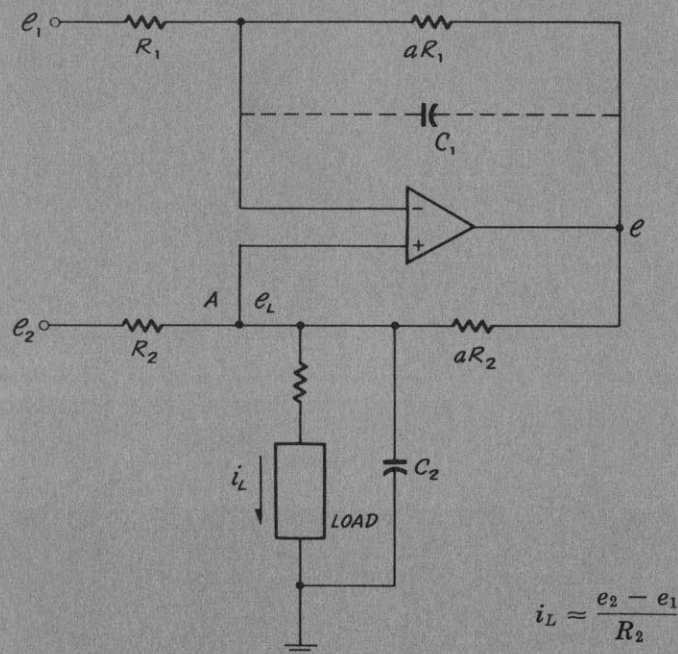
### III.6 CURRENT PUMP IV — GROUNDED SOURCE, GROUNDED LOAD.

The "Howland" circuit is made, as are most current sources, to approach infinite impedance by the application of positive feedback. The current through the load is given by:

$$i_L = \frac{e_2 - e_1}{R_2} \quad (3-2)$$

to an accuracy determined by the ratio of  $e_n$  to  $e_L$ , and by the ratio of the amplifier input current to  $i_L$ . In this circuit, both input voltages may be developed with respect to ground, and one side of the load may be conveniently grounded. Further, within the voltage and current capabilities of the amplifier, as with all of these circuits, both positive and negative currents may be driven through the load, depending only on the polarities of  $e_1$  and  $e_2$ .

Note that  $e_2$  supplies the short-circuit load current, whereas  $e_1$  need only supply the current to a network that may usually be made to have a relatively high impedance; therefore, when and if only one signal needs to be used, and when the available signal polarity is appropriate, it is preferable to ground  $e_2$  and use the  $e_1$  terminal as the current-determining input terminal.



$$i_L \approx \frac{e_2 - e_1}{R_2}$$

$$e = e_L + \frac{a}{1 + aR_1C_1p} (e_L - e_1)$$

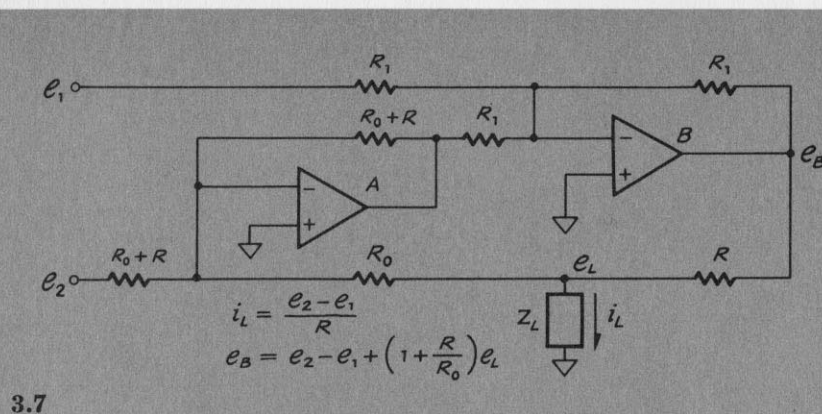
3.6

III.5  
I.7  
I.18  
I.34  
II.1  
to  
II.5  
III.3  
III.4  
III.6  
to  
III.9  
III.31  
III.38  
III.59

III.6  
I.7  
I.18  
I.34  
II.1  
to  
II.5  
II.28  
II.29  
III.3  
III.4  
III.5  
III.7  
III.8  
III.9  
III.31  
III.38  
III.59



**III.7 CURRENT PUMP V, CHOPPER-STABILIZED.** When it is desired to gain the advantage of chopper stabilization in constructing a current pump of the Howland Configuration, one must deal with the problem that chopper-stabilized amplifiers do not offer the necessary differential-input configuration. The circuit shown here is the functional equivalent of the Howland Circuit. Resistor  $R$  performs the current monitoring function, and the small drop across it is compensated for by increasing the feed-back resistor in amplifier  $B$  by the same amount, so that amplifier  $B$  has slightly higher than unity gain. This current pump is capable of extremely accurate control of the current through the load, and is usually limited in accuracy by the resistors involved, rather than by amplifier drift or uncertainty. Its speed of response may be very nearly the same as that of the circuit of III.6, all other things being equal. Since current pumps have essentially "infinite" internal impedance, if a voltage is applied to  $e_L$  ( $e_1$  and  $e_2$  at zero), its source will see a very high impedance, and the circuit will behave as a stabilized follower with gain having "push-pull" output at points A & B.



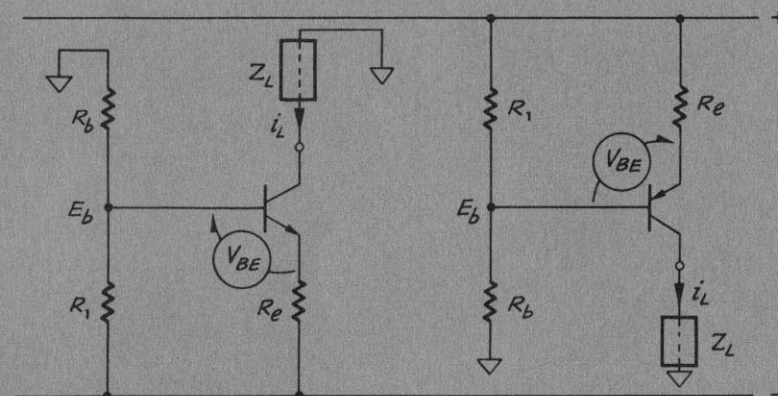
3.7

**III.8 CURRENT PUMP—SINGLE TRANSISTOR.** In the interest of objectivity, we feel it only fair to introduce, at this point, a pair of circuits in which some kind of current pump action may be achieved without benefit of an Operational Amplifier. These circuits are not eminently high-performance current pumps, and it frequently turns out that they are used in conjunction with Operational Amplifiers . . . which explains, perhaps, our gallant objectivity! Many applications will be found for these circuits in configurations that require relatively constant current, but in which current variations cause, at the most, second-order errors.

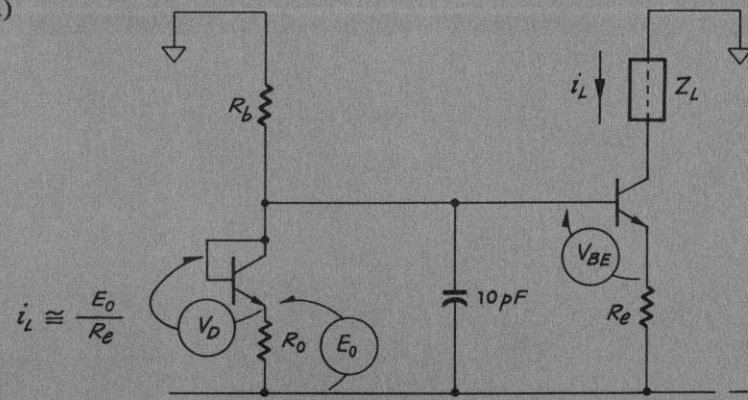
The circuits shown to the right behave identically in a complementary manner: as emitter-followers with the load to be driven connected into the collector-return circuit. The current level is established by setting the base voltage of the transistor,  $E_b$ , to an appropriate value—first by the resistance divider shown, or by furnishing an external signal of the required value. If  $E_b$  is large compared to the base-emitter drop of the transistor, then the current through  $R_e$  is approximately given by  $E_b/R_e$ . If the current gain,  $\beta$ , of the transistor is high enough, we may neglect the emitter-base current, and thus state that  $i_L$  is also approximately equal to  $E_b/R_e$ . The base-emitter voltage drop can be partially compensated if  $R_b > R_1$  by adding a diode in series with  $R_1$ , thus improving accuracy and providing first-order temperature compensation.

Provided that the available power supply can furnish the load voltage drop and  $E_b$ , leaving a volt or two for the emitter-to-collector voltage, and provided that the ratings of the transistor are not exceeded, this circuit, in all its approximate glory, functions as a current source of some utility. It is reasonably independent of the nature of the load—simple, complex, or active—and is certainly economical and straightforward.

It is doubtful whether an order of accuracy of better than 0.05% is worth attempting with this circuit.



3.8(a)



3.8(b)

FIRST-ORDER TEMPERATURE-COMPENSATED, NPN

III.7  
I.7  
I.18  
I.34  
III.3  
to  
III.9  
III.31  
III.38  
III.59

III.8  
I.45  
II.34  
II.35  
II.43  
II.44  
III.3  
to  
III.7  
III.9

**III.9 CONSTANT-CURRENT REGULATOR.** In this circuit, a unipolar derivative of the Howland circuit, a follower with gain is used to add or subtract a correcting current to or from (larger) unregulated current derived directly from the power supply through  $R_3$ . It must be appreciated that this circuit depends for its accuracy on the stability of the +15 volt supply with respect to signal ground . . . as well as the accuracy and stability of  $R_3$ ,\* and the accuracy and stability of the other resistors in the feedback networks.

Let us deal first with the diodes connected across the amplifier input terminals. They function merely as input signal clamps, preventing excessive input voltage in the event that the load is disconnected or suddenly becomes a very high impedance.

If  $R_2 = aR_1$ , and  $R_4 = aR_3$ , then it can be shown that in the ideal case the load current is simply given by  $i_L = 15/R_3$ .

The sources of error, beyond the resistor contributions and the power supply stability mentioned above are as follows: Input current to the amplifier; Voltage offset and drift; and CME and finite-gain error factors.

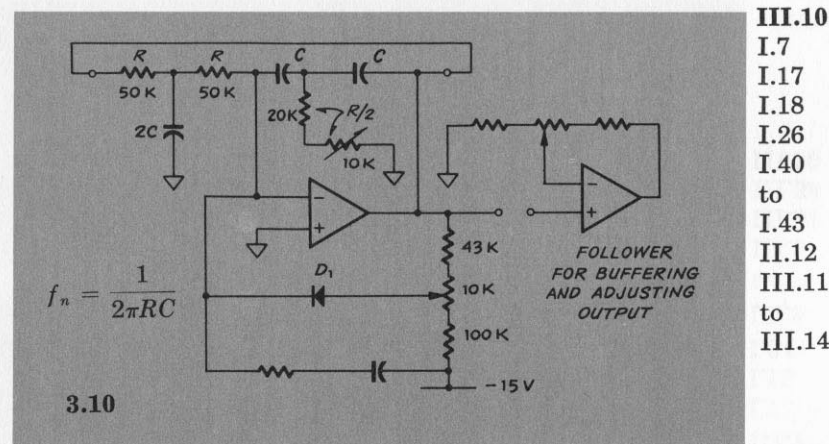
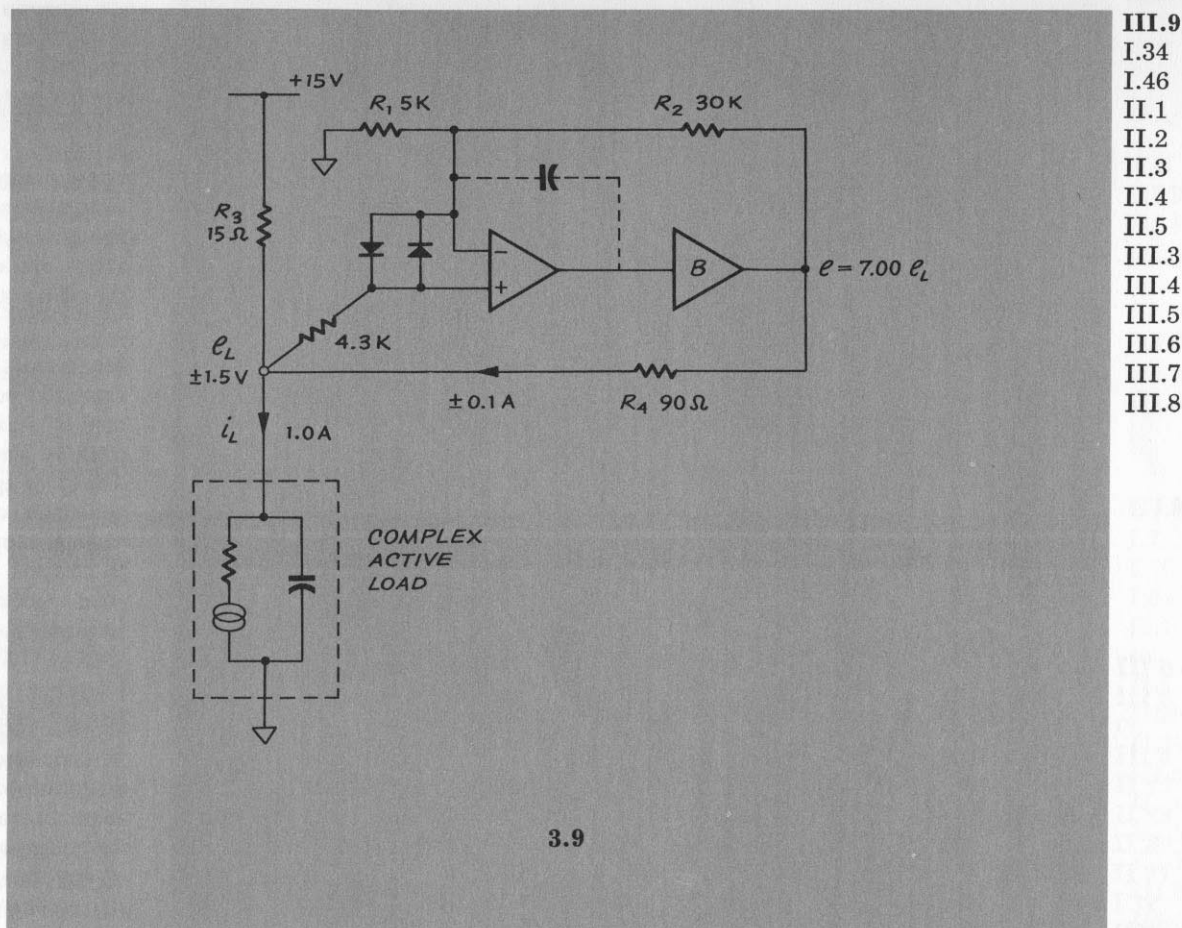
The booster current ratings should be selected to match the requirements of the load, and the output voltage capability of the booster must be such that it can furnish that current through  $R_4$ , when  $R_4$  is made equal to  $aR_3$ .

The 4.3 k $\Omega$  resistor shown in series with the positive input terminal in our example, is so proportioned (with respect to  $R_1$  and  $R_2$ ) as to reduce the effect of current offset. It also prevents excessive current in the clamping diodes.

\*Establishing high accuracy and holding high stability in a 15 $\Omega$  15-watt resistor may not be as easy as it sounds. Extreme derating helps, of course.

**III.10 SINE WAVE OSCILLATOR—TWIN-TEE.** This circuit is almost identical to the double integrator of II.14. At some frequency, when  $R/2$  is exactly 25 k $\Omega$ , the phase shift around the feedback loop is exactly 180°, so that the total phase shift, including the amplifier's sign inversion, is 360°, and the circuit is zero damped. A small increase in  $R/2$  will encourage oscillatory buildup. (Note that the accuracy of frequency and zero-ness of damping are encouraged if  $f$  is well within the amplifier bandwidth—see I.17 and I.41.) Without the damping network at the lower right of the diagram, sustained oscillations would build up between the extremes of saturation of amplifier—producing a distorted output. Beyond a selected threshold, a damping path

through the biased diode,  $D_1$ , maintains a stable, sinusoidal oscillation at a selected, adjustable value of peak-to-peak output. Adjusting the threshold will adjust the output. The voltage at which the damping circuit limits the amplitude is a direct function of power supply voltage, and is temperature-dependent because the diode forward voltage drop is. The series RC circuit from summing point to power supply can be proportioned for rapid startup yet minimal interference with normal operation. The output impedance of this circuit is, unfortunately, high near  $f_n$ ; therefore, this circuit would benefit from the addition of a follower or inside-the-loop booster. The follower choice allows adjustable output, as shown.

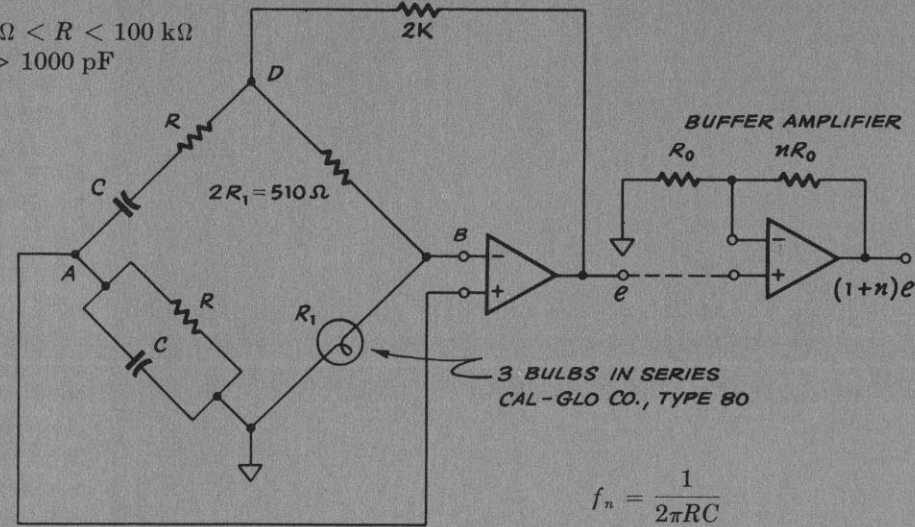




**III.11 SINE WAVE OSCILLATOR (Wien Bridge).** At the frequency  $f_n$ , the voltage at A is  $\frac{1}{3}$  of that at D, and in phase with it. The voltage at B is approximately the same, varying from slightly more than to slightly less than that at A, as the average power dissipated in  $R_1$  decreases. This variation at point B acts to regulate (without distorting) the output amplitude, which amplitude can be adjusted by setting  $R_2$  appropriately. At balance, there is no net feedback; hence the output impedance is high equalling that of the open-loop amplifier. As noted in III.10, an adjustable-gain buffering amplifier could be used as a convenient way to adjust the output amplitude.

$R_1$  actually consists of three incandescent lamps in series, operated below their visible-illumination current level. Because the regulating action of these lamps is primarily a thermal effect, the output amplitude of this circuit is inherently temperature-sensitive and it must be temperature-compensated (III.14) or oven-stabilized, if amplitude stability against ambient temperature is required. Over reasonable ranges, neither the amplitude nor the frequency of oscillation are affected by power supply variations.

$$1 \text{ k}\Omega < R < 100 \text{ k}\Omega \\ C > 1000 \text{ pF}$$



3.11

**III.12 TWO-PHASE OSCILLATORS.** Circuit (a) cascades a non-inverting integrator with a bounding inverting integrator, in a feedback loop represented by the differential equations:

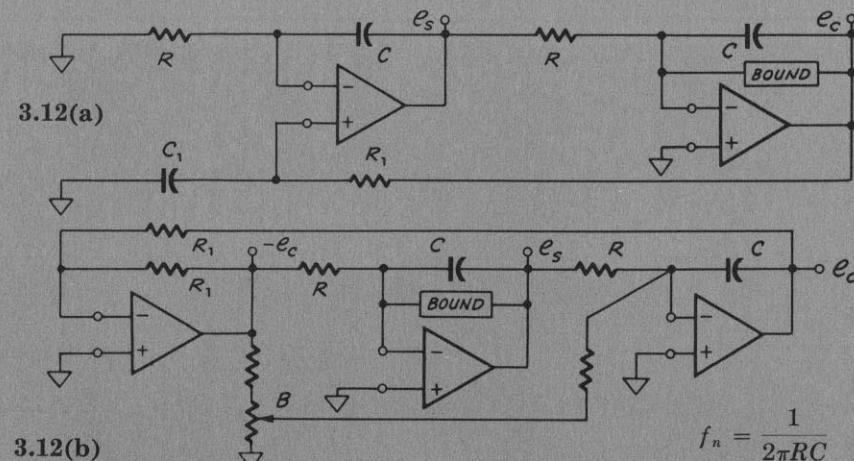
$$RC \frac{de_s}{dt} = e_c \quad RC \frac{de_c}{dt} = -e_s \quad (3-3)$$

The time constant  $R_1C_1$  is deliberately made slightly larger than  $RC$ , so that the circuit is slightly unstable; the bound stabilizes the amplitude without greatly distorting the waveform of  $e_c$ .\* Note, the two outputs are  $90^\circ$  out of phase.

$$e_s = E \sin \frac{t}{RC} \quad e_c = E \cos \frac{t}{RC} \quad (3-4)$$

Circuit (b) is similar, but employs inverting amplifiers only, thus enhancing its usefulness in very slow, very fast, and computer-bound applications, ... advantages implicit in the wider choice of available single-ended amplifiers. Positive feedback is provided at B to cause the oscillations to build up until bounded.

\*Because of the integration that operates upon  $e_c$ ,  $e_s$  will be nearly a perfect sinusoid.



3.12(b)

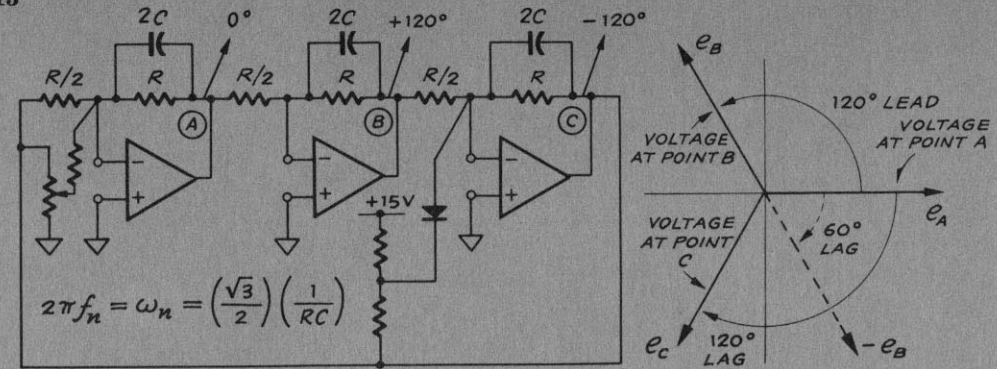
III.11  
I.7  
I.17  
I.18  
I.26  
I.40  
to  
I.43  
II.12  
II.21  
III.10  
III.12  
III.13  
III.14

III.12  
I.7  
I.17  
I.18  
I.26  
I.40  
to  
I.43  
II.12  
II.21  
III.10  
III.11  
III.13  
III.14

**III.13 3-PHASE OSCILLATOR.** This circuit produces three signals at the same frequency ( $f$ ) but phase-shifted  $120^\circ$  apart, one from the other. The total phase shift around the loop, at  $f$ , is  $360^\circ$ , each of the three identical "unit lags" contributing an effective  $120^\circ$  by combining its  $60^\circ$  lag and the normal polarity inversion of the amplifier, as shown in the vector diagram.

Note that the biased-diode amplitude-limiter circuit used previously in III.10 and III.12 is also employed here, as is an adjustment to permit setting the loop phase-shift just to the point of oscillation.

3.13



III.13  
I.7  
I.17  
I.18  
I.26  
I.40  
to  
I.43  
II.12  
II.21  
III.10  
III.11  
III.12  
III.14

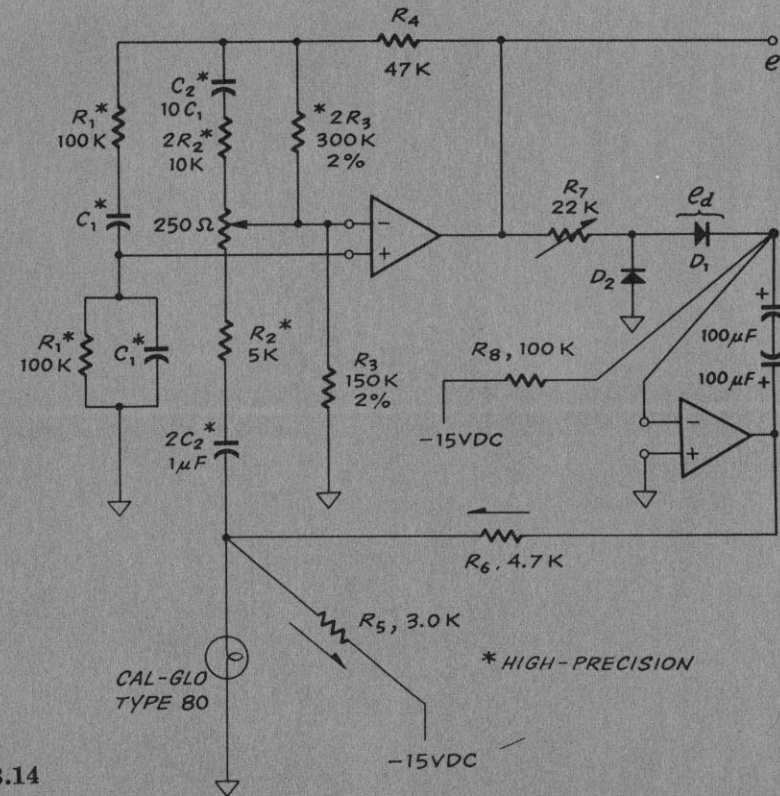
### III.14 WIEN BRIDGE OSCILLATOR—AMPLITUDE-CONTROLLED.

Very precise and stable control of the amplitude of a sine-wave Wien-bridge oscillator is achieved by the circuit shown here. The amplifier to the left oscillates when the positive feedback fraction of the output terminal exceeds the negative feedback fraction. The magnitude of the negative feedback signal is dependent upon a voltage divider, one element of which is an incandescent lamp. As the effective (RMS) current through the lamp increases, its resistance increases, increasing the negative feedback, reducing the amplitude of oscillation. The current in the lamp is derived from three sources: the current through  $R_6$  (DC) the current through  $R_5$  (DC from the  $-15$  volt supply) and the current through  $C_2$ ,  $R_2$ , etc. divider (AC at the oscillator frequency).

An integrator circuit drives  $R_6$ . The input to this integrator is a half-wave-rectified current derived from the output sine-wave through  $R_7$  and  $D_1$ . ( $D_2$  clips the negative half-cycle.) By so proportioning  $R_7$  and  $R_8$  that the average net input current at the summing point of the integrator is effectively zero when the output amplitude is at the desired value, and by adjusting the time constant of the integrator to filter the rectified sine-wave effectively, the output voltage of the integrator will be essentially DC, and will be essentially zero when, and only when, the output amplitude is correct.

If the output amplitude should fall, the integrator output would swing positive, driving a positive current through  $R_6$ , reducing the net current through the lamp, since this current would furnish some of the current demanded by  $R_5$ . If the output amplitude should rise, the integrator output would go negative, increasing the current through the lamp. Both actions will be seen to operate so as to regulate the sine-wave output. Since the gain of the integrator is quite high, it permits only a very small variation in the output amplitude. To avoid low-frequency oscillation, or "hunting," the integrator time constant must be somewhat longer than the lamp time constant.

3.14



III.14  
I.7  
I.17  
I.18  
I.26  
I.40  
I.41  
I.42  
I.43  
II.12  
II.21  
III.10  
III.11  
III.12  
III.13

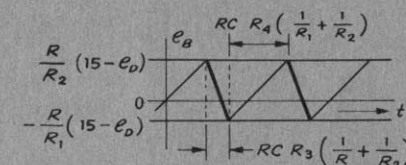
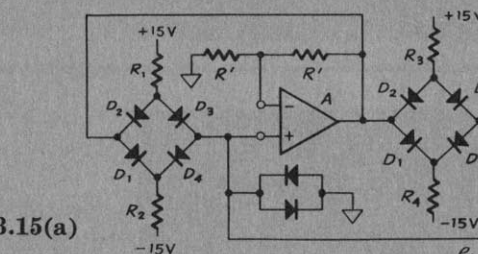


**III.15 PRECISE TRIANGULAR-WAVE GENERATOR.** The output of amplifier A switches between  $\pm 1$  volt (approximately) levels determined by the two diodes clamping the positive input to ground. Amplifier A drives two current gates (diode bridges) so arranged that when  $e_A$  is positive,  $D_1$  and  $D_3$  conduct, while  $D_2$  and  $D_4$  block. This circuit condition connects  $+15$  V through  $R_3$  to the summing point of amplifier B, an integrator. The output of B is, in this mode, a negative-going ramp, the magnitude of which continues to increase until it is large enough to drive the input of amplifier A negative, causing the output of A to flip. (The switching speed can be extremely high, if amplifier A is fast.)

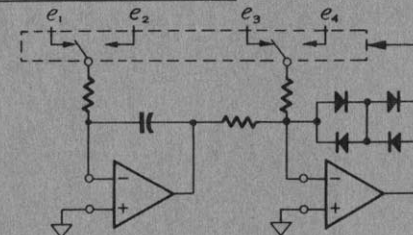
After amplifier A flips, the behavior of the circuit is reversed throughout:  $-15$  V is connected, through  $R_4$ , to the summing point of integrator B; the output of B is a positive-going ramp, continuing until it drives the input of A positive, causing the output of A to flop back to the state it had at the start of this description.

This circuit can perform well at frequencies ranging from  $10^{-3}$  Hz to  $10^6$  Hz, depending upon the choice of amplifier, diode, and impedance levels.

3.15(a)



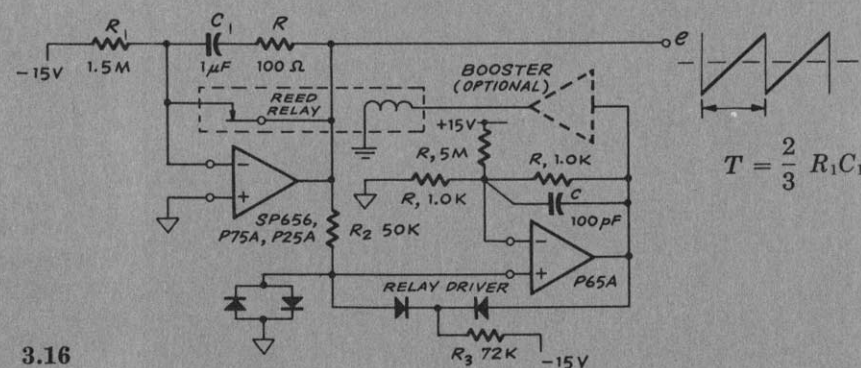
3.15(b)



3.15(c)

**III.16 PRECISE SAW-TOOTH GENERATOR, LOW FREQUENCY.** The input signal to the integrator is the  $-15$  V reference. When the output voltage has reached  $+10$  volts, the current through  $R_2$  balances the current through  $R_3$ , the voltage at the positive input of the relay driver becomes positive, and the relay driver switches its output from (about)  $-1$  volt to (about)  $+1$  volt, driving the reed relay to reset the integrator. (If a Philbrick SPREL is used, no booster is necessary, as it requires only a  $+1$  volt or  $-1$  volt logic level to activate a high-reliability reed relay.) When  $e$  has arrived at zero, the relay driver senses this (because  $R_3$  has been effectively disconnected) and its output switches back to  $-1$  volt, removing the excitation from the reed relay reconnecting  $R_3$ , and starting the cycle again.

3.16



III.15  
I.25  
I.27  
II.10  
II.11  
II.12  
II.39  
II.41  
II.43

III.16  
I.24  
I.25  
II.10  
II.11  
II.12  
II.41

**III.17 ASTABLE (FREE RUNNING) MULTIVIBRATOR.** This circuit has two metastable states, in one of which the output is at positive saturation, and in the other of which the output is at negative saturation. The circuit regularly shifts from one to the other of these two states; hence, the output is a square wave, the period of which is determined by the values of  $R$  and  $C$ , and by the feedback ratio established by the output divider that drives the positive input terminal.

Assume that the amplifier saturates symmetrically at  $\pm 12$  volts output, and let us begin our analysis by assuming that the circuit has been in its positive-output state long enough for the capacitor  $C$  to have charged sufficiently so that the potential at the negative input terminal has just approached the potential of the positive input terminal. At (or immediately after) the instant at which they become equal in potential, the circuit will switch, very rapidly, from its positive-output state to its negative-output state.

In the new state, the positive input terminal is held at a potential of about  $-1.1$  volt. The negative input terminal is still connected to the capacitor  $C$ , which has had no opportunity to change its voltage, and is still charged to  $+1.1$

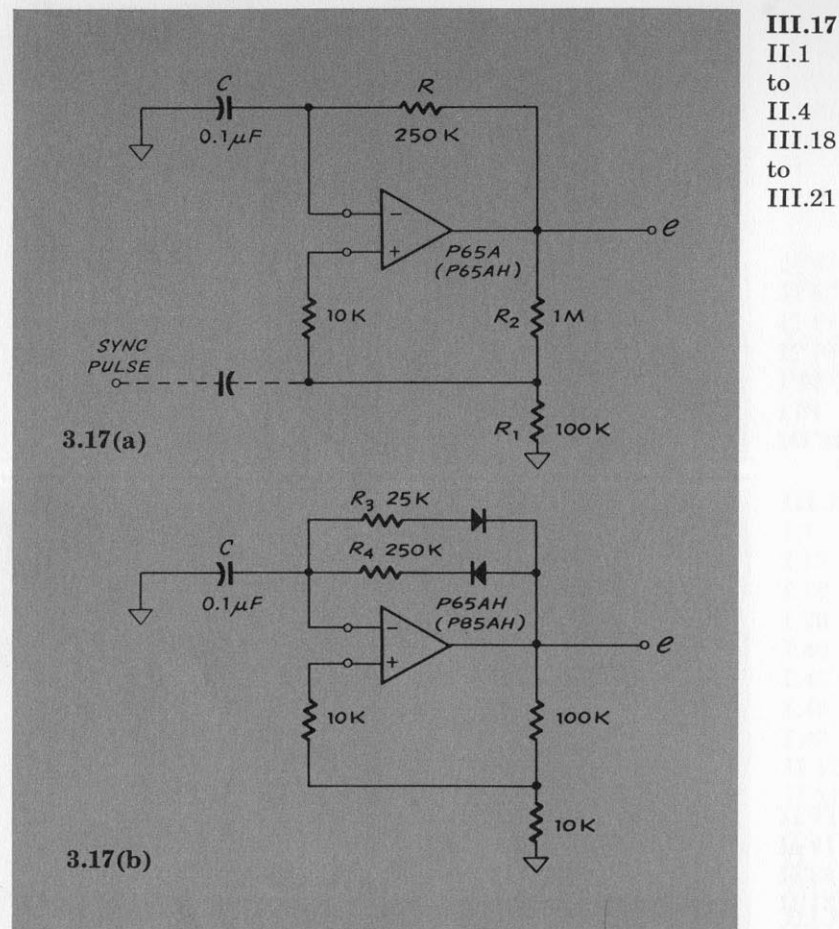
volts, because the switching action occurs essentially instantaneously. The circuit remains locked, therefore, in the negative-output state for the period of time that is required for  $C$  to discharge and re-charge to approximately  $-1.1$  volts, through  $R$ . This time interval, obviously, is dependent on the product of  $R$  and  $C$ : The fact that the voltage across  $C$  must change by a total of  $2.2$  volts is determined, of course, by the  $1:11$  ratio of the output divider . . . if the divider had had a different ratio, the voltage difference through which the potential of the negative terminal would have had to swing would have been different, also. The exact expression for the operating frequency is:

$$f = \frac{1}{2RC \ln \left( 1 + 2 \frac{R_1}{R_2} \right)} \quad (3-5)$$

Note that if, during the time that  $C$  is charging to the new value required for the circuit to switch states, a large enough pulse (of the opposite polarity to the output) is fed into the synchronizing terminal, the circuit will immediately change state. The frequency is essentially independent of loading or power supply voltage.

**III.18 SIMPLE SQUARE WAVE GENERATOR.** The output of this circuit is limited by a pair of back-to-back zener diodes which, beyond their avalanche voltage limits, exhibit such low impedance compared to the output impedance of the circuit that they ensure generation of a clean, flat-topped wave by "clipping" the output below the amplitude at which overshoot, ringing, or rounding can occur. The positive input terminal of the amplifier is connected to an output divider that provides positive feedback. Suppose that the output is at  $+E_z$ . The positive input terminal will be at about  $+11/26 E_z$ .

Capacitor  $C$  will be charged via  $R$  until the voltage at the negative input exceeds  $+11/26 E_z$ . Because of the amplifier's high gain, the output  $e$  will "flip" to  $-E_z$ . The positive input will be at  $-11/26 E_z$ , maintaining the saturated condition. The capacitor  $C$  will start to charge exponentially in the negative direction (from  $+11/26 E_z$  to  $-E_z$ ), and the output will flip once again when the output crosses  $-11/26 E_z$  starting the cycle again. The positive feedback aids in driving the circuit more rapidly to saturation; the  $2.4 \text{ k}\Omega$  resistor limits the amplifier current during clipping to within  $2 \text{ mA}$ .

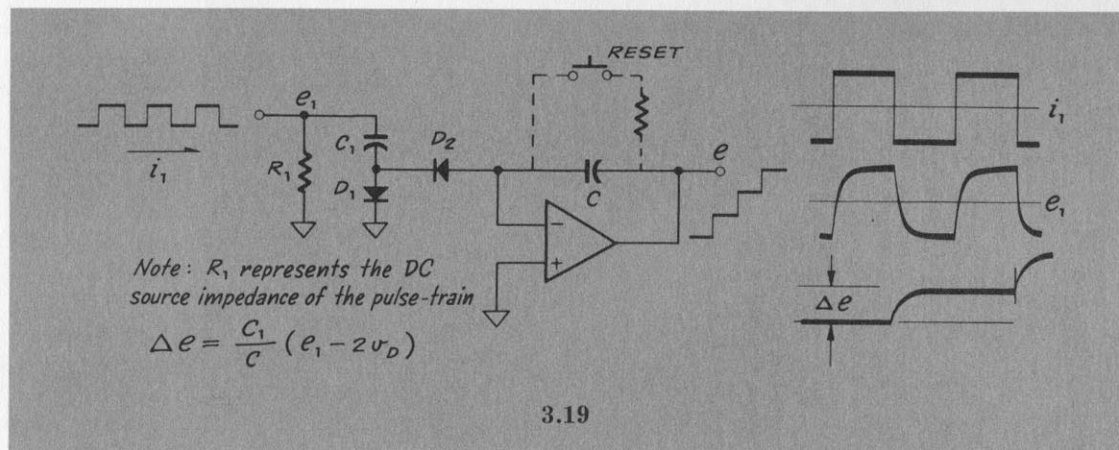


III.17  
II.1  
to  
II.4  
III.18  
to  
III.21

III.18  
II.1  
II.2  
II.3  
II.4  
III.17  
III.19  
III.20  
III.21



**III.19 STAIRCASE GENERATOR.** This circuit must be driven from a current source. Each positive upstep charges  $C_1$  through  $D_1$ . The corresponding negative downstep discharges  $C_1$  (in parallel with the source resistance, if DC coupled) through  $R_1$  and  $D_2$ , drawing current from the summing point. This current must, of course, come from the capacitor  $C$ . Thus, a series of current pulses are drawn through  $C$ , and the voltage across  $C$  (the output voltage,  $e$ ) increases by the time-integral of each of those current pulses. If the  $R_1C_1$  time constant is short compared to the pulse-to-pulse spacing, the output wave form will resemble a staircase, as shown. The circuit may be reset by means of a pushbutton . . . or if manual reset is not practical, by means of a relay operated from the generator output, at some critical value of time or output voltage—the last desired “step.”



III.19  
II.1  
to  
II.4  
II.10

### III.20 BISTABLE MULTIVIBRATOR.

These circuits are different forms of bistable multivibrators, frequently miscalled “flip-flops.” Each has two stable states, in either one of which it will remain indefinitely, unless and until a step or pulse signal of appropriate polarity is fed to the input, to change its state.

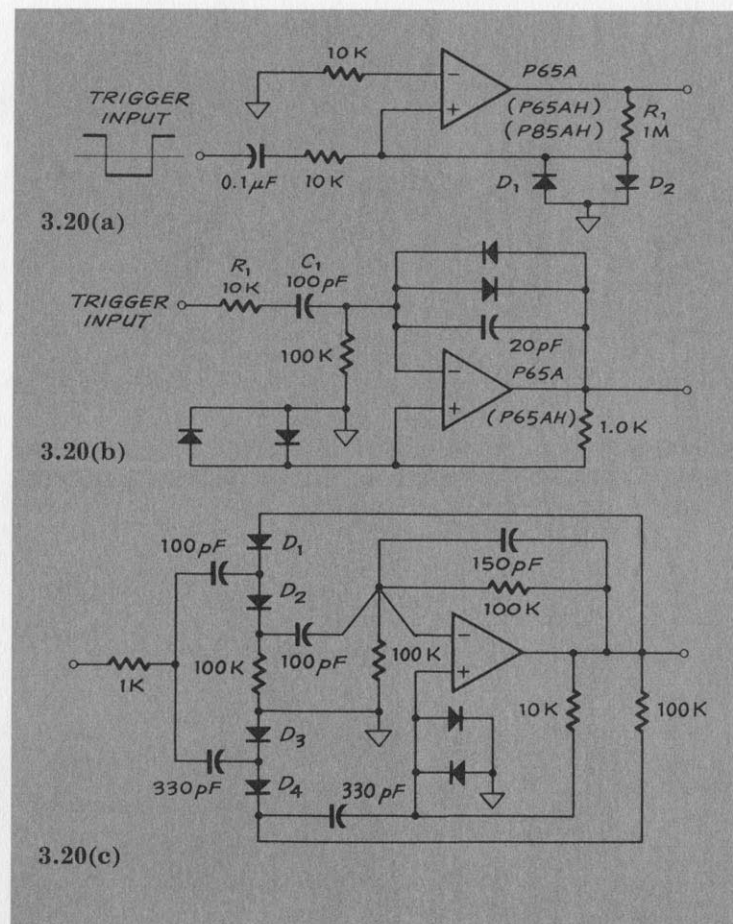
In the basic (saturating) circuit of (a), the output is saturated at either its positive or its negative limit (typically  $\pm 12$  V) because of the positive feedback to the positive input through  $R_1$ . A small step of opposite polarity applied to the trigger input will reverse the polarity of the voltage at the positive input. Within a millisecond the output will switch to its other limit, and the positive feedback via  $R_1$  will keep it there, until a step of the opposite polarity is applied to the trigger input. Square waves, pulses, sine-waves, from 1.0 V to 20 Vp-p, and from very low frequency to a few hundred cycles per second will activate the circuit.

The circuit shown in figure 3.20(b) uses diode bounding to prevent saturation. Its two stable

output states are +1 V and -1 V. It is more sensitive than the circuit in 3.20(a), and will respond faster, even to smaller input signals. With the values shown, square waves, etc., as small as 0.1 Vp-p, and as fast as 20 kHz will reliably switch the state of the circuit. If the existing trigger signal is substantially larger than 0.2 Vp-p,  $R_1$  may be increased and  $C_1$  decreased, to minimize the loading on the trigger signal source.

The circuit in figure 3.20(c) is a special kind of bi-stable device that changes state only every other cycle of input, and thus can be used as a frequency divider or scale of two counter. The diode steering networks  $D_1$ – $D_4$  insure that negative-going steps are steered alternately to the positive and negative inputs. With the values shown, square waves of 1 to 4 Vp-p, and from very low frequencies to 10 kHz will actuate the circuit.\* Of course, any number of (c) circuits may be cascaded, to achieve (binary) frequency division or counting with moduli of 2, 4, 8, 16, or more.

\*with outputs up to 5 kHz.



III.20  
III.17  
III.18  
III.21

**III.21 MONOSTABLE MULTIVIBRATOR.** A monostable multivibrator has only one stable state. However, immediately following the introduction of a trigger pulse, it will change state and stay in the new “metastable” state for a predetermined period, and then return to its stable state.

In circuit (a), the output states are plus and minus saturation (+12 V and -12 V, typically). When a negative step is applied to the trigger input (3 to 8 volts, typically) the output switches from its stable state at +12 V to -12 V, and  $R_f$  begins to charge  $C_1$  toward -12 V. When the voltage on  $C_1$  reaches a point at which  $|e_B| > |e_A|$ , the amplifier output voltage switches back to +12 V, and will remain there until the circuit is triggered again. Meanwhile, the voltage on  $C_1$  starts to charge back up from -1 V to +12 volts, but is clamped at about +0.6 V, by  $D_1$ . Values of  $C_1$  from 1000 pF to 10  $\mu$ F and of  $R_f$  from 10 k $\Omega$  to 2 M $\Omega$  are suitable (for smaller values of  $R$  or  $C$ , a fast amplifier is recommended). With the values shown, the temporary state lasts about 1 second.

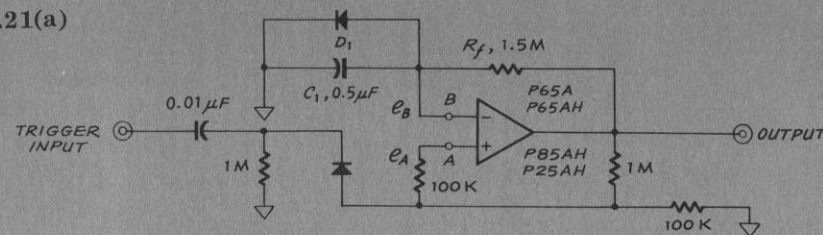
To obtain more predictable and “nearer-ideal” behavior, circuit 3.21 (b) is recommended. As in the nonsaturating flip-flop of 3.17(b), diode bounds are used to prevent saturation and improve response speed, trigger sensitivity, and stability. The circuit is a variation of the triangular-wave generator of III.15. In the stable state, the switch output is at about -1 VDC, and about 0.5 mA flows through  $D_4$  and  $D_5$ . The integrator’s output is bounded at about 0 V by  $D_5$ .

If a step signal of sufficient magnitude is applied to the trigger input, the output of the switch will go very quickly to +1 volt. Current then flows through  $R_1$  and  $D_2$ , and the output of the integrator begins to ramp downward linearly. When it reaches -10 volts, the current through  $R_4$  balances that through  $R_3$ , and the switch flips back to its permanent state of -1 V. This connects  $R_2$ , through  $D_4$  resetting the integrator. Since  $R_2$  can be much smaller than  $R_1$ , the reset can be accomplished quickly. Using the formula

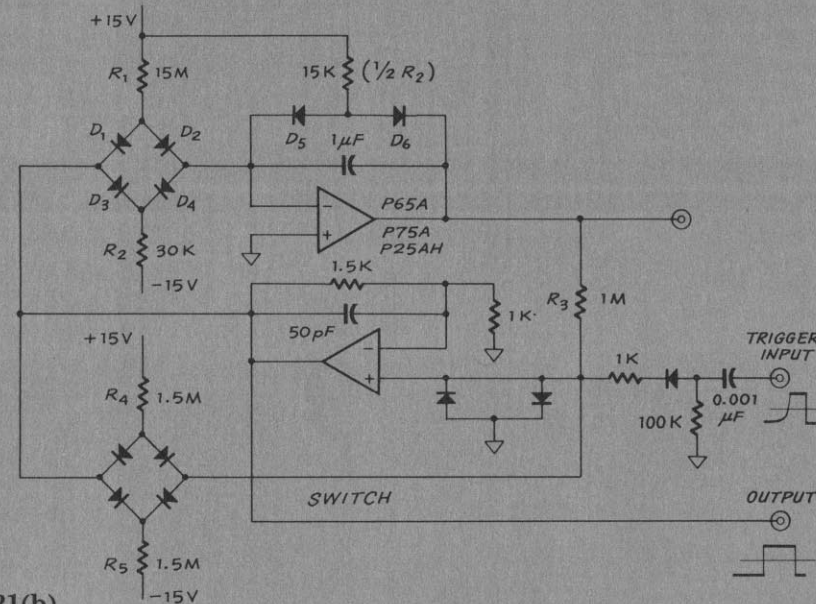
$$\tau = 0.7R_1C \quad (3-6)$$

for the component values shown, the output will be at +1.0 volt for 10 seconds. Substituting the value of  $R_2$  for  $R_1$  in equation (3.6) gives the formula for the reset time—in this example, only 20 milliseconds.

3.21(a)



3.21(b)

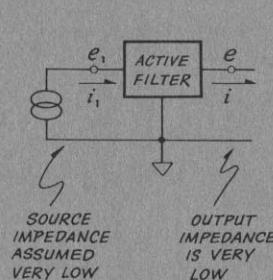


**III.22 ACTIVE FILTERS.** Operational Amplifiers can greatly simplify the design of high-performance signal filters, because they eliminate the need for inductors and for impedance matching. Furthermore, use of active filters can result in reduction of weight, size, and cost. Filters designed to satisfy sophisticated mathematical criteria can be realized without resort to “equalization” or trimming.

We shall, in the six sections that follow, attempt to summarize a two-part article published in *The Lightning Empiricist*, Vol. 13, 1 & 2, 3 & 4. Our necessarily brief considerations will include Operational Amplifier circuits for low-pass, high-pass, band-pass, and band-reject filters. Procedures for cascading quadratic filter stages will be presented, so that high-order “mathematically-designed” filters, in this case the Butterworth, may be synthesized.

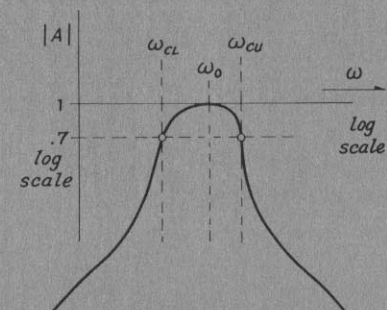
In section III.28, we present (in highly-concentrated form) filter-design tables and a design example, all from the second part of the article, in which all these matters are examined in a less compressed, more detailed manner.

3.22



$$e = A\{p\}e_1$$

$$pe_i \equiv \frac{de_i}{dt}$$



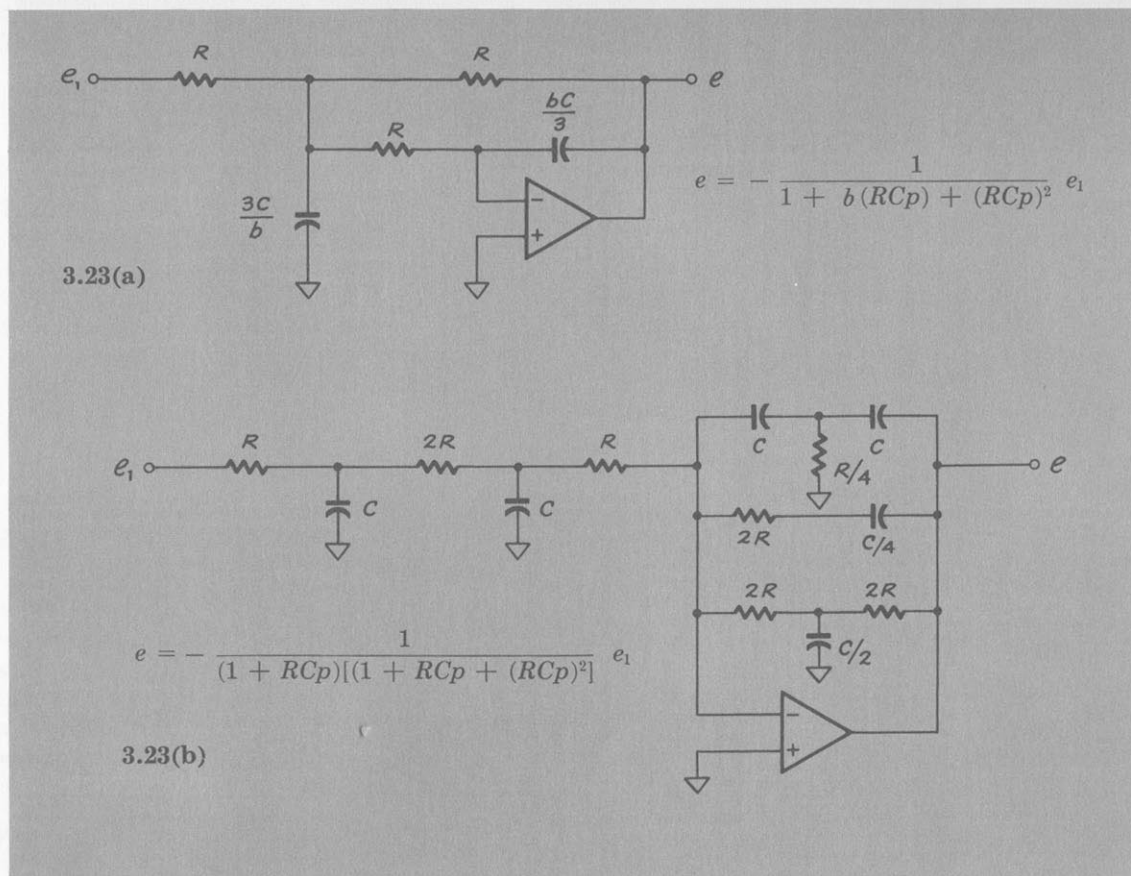
$$\omega_0 = \sqrt{\omega_{CU}\omega_{CL}}$$

$$B = \frac{\omega_{CU} - \omega_{CL}}{2\omega_0}$$



**III.23 SIMPLE LOW-PASS FILTERS.** The simplest of low-pass filters are the first-order lag circuits of II.15 and II.16. *Efficient* higher-order filters exhibit a response equation having no more than one real root, the other factors being damped quadratics ( $b < 2$ ). Figure (a) shows a typical quadratic or second-order underdamped filter section. Several such sections may be cascaded to achieve a higher even-order (e.g., 4th, 6th, etc.) filter characteristic.

An example of a third-order filter circuit was given in II.18. Another is shown in (b). This circuit is a third-order Butterworth filter having relatively sharp cut-off and a flat band-pass region. Its response is 3 db down at  $\omega = \frac{1}{RC}$  rad/sec. Another useful third-order filter is shown in III.69.



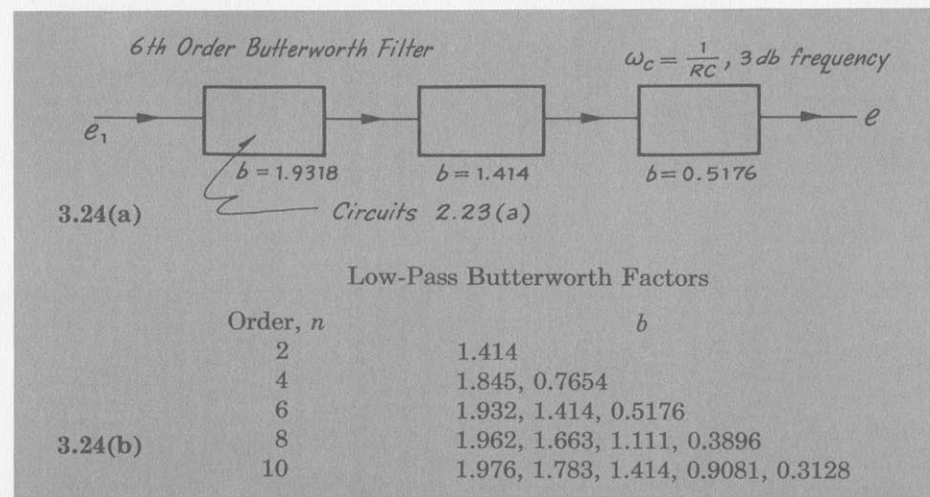
**III.24 CASCADING ACTIVE FILTER SECTIONS.** Cascading quadratic factors as indicated in (a) is an efficient way of achieving a filter with very high-performance characteristics, particularly when dealing with low-pass and band-pass designs. There is no need for the sections to be identical; in fact,

Butterworth low-pass factors all have unique damping ratios ( $\frac{b}{2}$ ) and narrow-band-pass factors all have unique natural frequencies and damping ratios.

Values of  $b$ , the damping ratio, are tabulated in Table (b) for various even-order low-pass Butterworth filters. The absolute value of the gain,  $|A|$ , for these filters is given (as a function of frequency,  $\omega$ ) by:

$$|A|^2 = \frac{1}{1 + (\omega RC)^{2n}} \quad (3-7)$$

The transient response of the Butterworth low-pass filter deteriorates in fidelity as the number of sections increases.



III.23  
II.1  
to  
II.4  
II.15  
to  
II.18  
III.22  
III.24  
to  
III.28

III.24  
II.1  
to  
II.4  
II.15  
to  
II.18  
III.22  
III.23  
III.25  
III.28

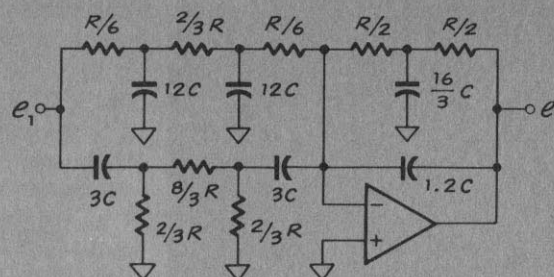
**III.25 “AVERAGING” FILTERS.** Circuit (a) is a modification of the third-order, linear-phase-shift (Paynter) filter shown in II.18. This has a notch at  $\omega = \frac{1}{RC}$ ,

achieving the amplitude vs. frequency characteristic shown in the heavy line in (b). The dotted line is the “ideal running-average” operator given by:

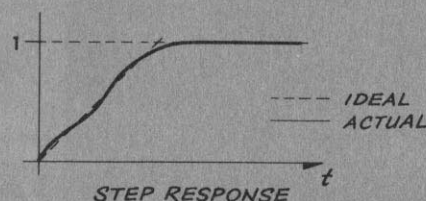
$$y = \frac{1}{T} \int_{t-T}^t x(t) dt = \frac{1 - e^{-Tp}}{Tp} \quad (3-8)$$

where  $T = \pi RC$ . Figure (c) compares the actual response (to a step input) with the ideal.

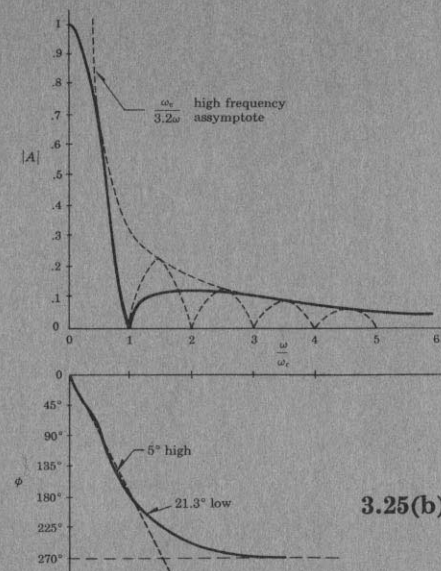
This filter is particularly useful for averaging functions of non-stationary random variables, since its transient-response time is minimum for a given averaging time.



3.25(a)



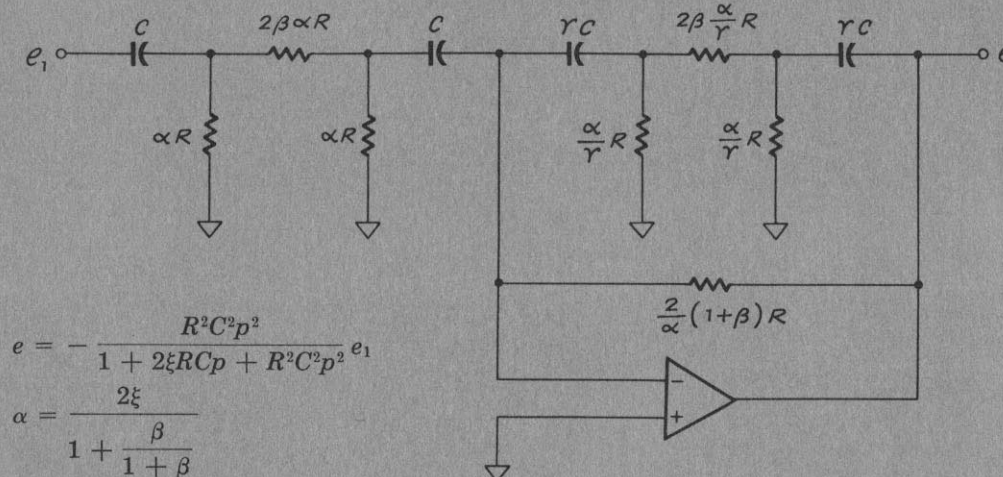
3.25(c)



3.25(b)

**III.26 HIGH-PASS FILTERS.** By applying a conformal transformation to a low-pass filter characteristic it is possible to convert that characteristic to a high-pass, band-pass, or band-reject characteristic having exactly the same gain and phase as the low-pass at corresponding frequencies. (The chart of Section III.28 lists these transformations.)

The high-pass characteristic achieved by this conformal-transformation process can be very effective at removing all frequency components below the cut-off frequency, while passing without attenuation all frequencies above cut-off; however, if the signal has significant frequency content in the neighborhood of cut-off, the resulting transient response does not permit good reproduction of the original waveform, due to phase distortion. The filter producing the least phase shift at the cut-off frequency is the first-order lead circuit shown in II.16. Another effective high-pass circuit is shown in the figure. This can be used as the quadratic factor (second-order section) of high-order filters. Remember that the amplifier gain-bandwidth limitation ultimately limits the high-frequency pass band. Depending upon the amplifier used, small feedback capacitors may be necessary to achieve stability.



$$e = - \frac{R^2 C^2 p^2}{1 + 2\xi RCp + R^2 C^2 p^2} e_1$$

$$\alpha = \frac{2\xi}{1 + \frac{\beta}{1 + \beta}}$$

$$\gamma = 1 - \frac{\frac{\beta}{1 + \beta}}{\left(1 + \frac{\beta}{1 + \beta}\right)^2} (2\xi)^2$$

$\beta$  chosen to avoid capacitive load  
make  $\beta \ll 1$  to minimize noise gain

3.26

III.25  
II.1  
to  
II.4  
III.22  
III.23  
III.24  
III.26  
III.27  
III.28

III.26  
II.1  
to  
II.4  
III.22  
to  
III.25  
III.27  
III.28



**III.27 BAND-PASS AND BAND REJECT (NOTCH) FILTERS.** A band-pass filter has two cut-off frequencies. Below the lower,  $\omega_{CL}$ , and above the upper,  $\omega_{CU}$ , signal components are highly attenuated. Between the two cut-off frequencies, the signal components are passed with nearly unity gain, and with phase shift varying significantly with frequency. To simplify calculation, it is convenient to define two terms:

$$\omega_0 = \sqrt{\omega_{CU}\omega_{CL}}, \text{ "center frequency"} \quad (3-9)$$

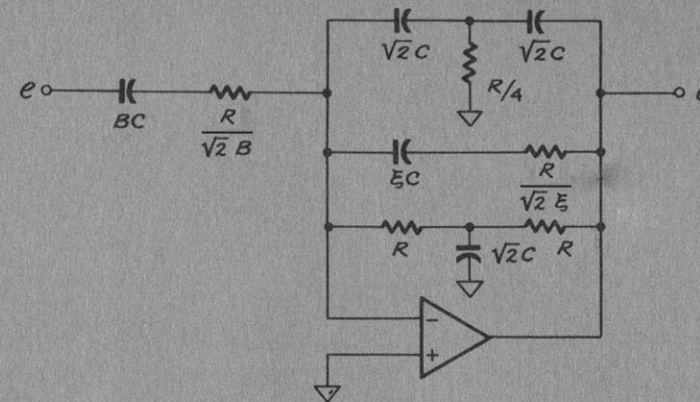
$$B = \frac{\omega_{CU} - \omega_{CL}}{2\omega_0}, \text{ "normalized bandwidth"} \quad (3-10)$$

We classify those band-pass filters having a  $B \geq 1$  ( $\omega_{CU}/\omega_{CL} > 6$ ) as "wide-band" and those with  $B < 1$  ( $\omega_{CU}/\omega_{CL} < 6$ ) as "narrow-band."

To get a wide-band-pass filter, we cascade a high-pass filter with cut-off at approximately  $\omega_{CL}$  with a low-pass filter with cut-off at approximately  $\omega_{CU}$ . The transformation listed in the Chart of III.28 yields a band-pass characteristic that is symmetrical about  $\omega_0$ , when plotted on logarithmic coordinates. Circuit 3.23(a) is typical of the low-pass filters used, and circuit 3.26 is typical of the high-pass filters one would cascade with them, to achieve a wide-band-pass characteristic.

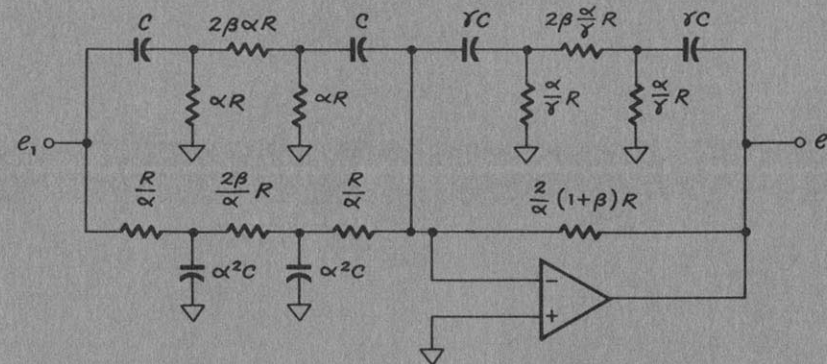
Narrow band-pass filters are used primarily for spectrum analysis. An active filter can be designed to respond to an extremely small band of frequencies, while rejecting all other components. When  $B$ , the normalized bandwidth, is very small, the damping ratio of each band-pass quadratic factor is also very small. This causes the filter to have a very slow transient response when a sudden change in spectral density of the input signal occurs. Circuit (a) is typical.

A band-reject filter, like the band-pass filter, has two cut-off frequencies. Between these two frequencies,  $\omega_{CL}$  and  $\omega_{CU}$ , signal components are heavily attenuated, whereas outside this band they are passed without significant attenuation. The same terms,  $\omega_0$  and  $B$ , are used in the design equations given in the Chart of III.28. Circuit (b) is typical; note the similarity to 3.26.



3.27(a)

$$e = \frac{2BRCp}{1 + 2\xi RCp + R^2C^2p^2} e_1$$



3.27(b)

$$e = -\frac{1 + R^2C^2p^2}{1 + b_1RCp + b_2R^2C^2p^2} e_1$$

$$\gamma = b_2 - \frac{\beta}{\left(1 + \frac{\beta}{1 + \beta}\right)^2} b_1^2 \quad \mu = \frac{b_1}{1 + \frac{\beta}{1 + \beta}}$$

$\beta$  chosen to prevent capacitive load problems  
(Make  $\beta \ll 1$  to avoid noise gain problems)

III.27  
II.1  
to  
II.4  
III.22  
to  
III.26  
III.28

**III.28 FILTER DESIGN DATA.** With Table (a), any of the first-order or second-order low-pass filter-circuits described and shown in III.23 may be used to predict the behavior of high-pass, band-pass, or band-reject filters of equivalent (conforming) design, as mentioned in III.26.

Table (b) summarizes the transfer functions of Butterworth and Paynter filters. For higher-order Butterworth factors, refer to III.24.

The following example illustrates the use of the chart:

**Task:** Design a band-pass filter, of the Butterworth Type, having a  $\frac{1}{2}$  octave effective noise bandwidth centered at 1 radian/second ( $\omega_0$ ), to be used for spectral power density measurement. The filter is to have a very sharp cut-off, such that at  $\omega = \sqrt{2}$  radians/second (the next highest center frequency in a comb filter), the gain is less than 0.1.

#### Procedure

##### Step 1. Determine B

Let  $\omega_{CU} - \omega_{CL} = 3$  db bandwidth.

$$B \equiv \frac{\omega_{CU} - \omega_{CL}}{2\omega_0}, \quad \omega \equiv \sqrt{\omega_{CU} \omega_{CL}} = 1 \text{ rad/sec}$$

Let noise bandwidth  $b_N = \omega_{CU}' - \omega_{CL}'$

such that  $\omega_0 = \sqrt{\omega_{CU}' \omega_{CL}'} = 1 \text{ rad/sec}$

For a half octave noise bandwidth:  $\frac{\omega_{CU}'}{\omega_{CL}'} = \sqrt{2}$

$$\text{Hence: } \frac{\omega_{CU}'}{\omega_0} = \frac{\omega_0}{\omega_{CL}'} = \sqrt[4]{2}$$

$$\text{Call: } K = \frac{2\pi b_N}{\omega_{CU} - \omega_{CL}} = \frac{\text{noise bandwidth}}{3\text{db bandwidth}}$$

Values of K are presented in Table 3.

$$K = \frac{\omega_{CU}' - \omega_{CL}'}{\omega_{CU} - \omega_{CL}} = \frac{\frac{\omega_{CU}'}{\omega_0} - \frac{\omega_{CL}'}{\omega_0}}{2 \frac{\omega_{CU}' - \omega_{CL}'}{2\omega_0}} = \frac{\sqrt[4]{2} - \frac{1}{\sqrt[4]{2}}}{2B}$$

$$\text{Hence: } B = \frac{\sqrt[4]{2} - \frac{1}{\sqrt[4]{2}}}{2K} = \frac{.174}{K}$$

**3.28(a)**

Step 2. Determine attenuation at  $\omega = \sqrt{2}$  rad/sec using table (a)

$$\begin{aligned} \text{Low Pass } \frac{\omega_L}{\omega_c} &= \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \frac{1}{2B} \\ &= \left( \sqrt{2} - \frac{1}{\sqrt{2}} \right) \frac{1}{2B} = \frac{\sqrt{2}}{4B} \end{aligned}$$

From table (b) the gain of the low-pass Butterworth filter is:

$$|A|^2 = \frac{1}{1 + \left( \frac{\omega_L}{\omega_c} \right)^{2n}} = \frac{1}{1 + \left( \frac{\sqrt{2}}{4B} \right)^{2n}}$$

Using the result of step 1 and values of K from the second L.E. filter article (Vol. 13, No. 3 & 4)

Order, (2n)	K	B	A
2	1.571	.111	.30
4	1.111	.157	.20
6	1.047	.166	.10 ← use

Step 3. Determine the transfer functions. Transforming the 3rd Order low-pass Butterworth Table (b) model using Table (a) gives:

$$e = \left[ \frac{2B \frac{p}{\omega_0}}{1 + 2B \frac{p}{\omega_0} + \left( \frac{p}{\omega_0} \right)^2} \right] \left[ \frac{2B \frac{p}{\alpha \omega_0}}{1 + 2\xi \frac{p}{\alpha \omega_0} + \left( \frac{p}{\alpha \omega_0} \right)^2} \right] \left[ \frac{2B \frac{\alpha p}{\omega_0}}{1 + 2\xi \frac{\alpha p}{\omega_0} + \left( \frac{\alpha p}{\omega_0} \right)^2} \right] e_1$$

where:  $\omega_0 = 1 \text{ rad/sec}$   
 $B = .166$

$$\alpha = \frac{1 + \frac{B \sqrt{1 - \xi_L^2}}{2}}{B \sqrt{1 - \xi_L^2}} = 1.155 (*)$$

$$\xi = \frac{2\xi_L B}{\alpha + \frac{1}{\alpha}} = .0822 \quad (\text{See Table a})$$

$$\xi_L = .5 \quad (\text{See Table b})$$

(\*) This approximation of the  $\alpha$  definition equation, Table (a), can be used when  $B < 1$ .

**3.28 (b)**

The circuit of Figure 3.27(a) can be used for each of the quadratic factors. Arbitrarily we can select the largest capacitor,  $\sqrt{2}C$ , to be a convenient value, 1  $\mu\text{F}$ .

Table a. TRANSFORMATIONS OF LOW PASS FILTERS

LOW PASS	HIGH PASS	BAND PASS	BAND REJECT
Mapping Relation			
$\frac{p_L}{\omega_c}$	$\frac{\omega_0}{p}$	$\left( \frac{p}{\omega_0} + \frac{\omega_0}{p} \right) \frac{1}{2B}$	$\frac{2B}{\left( \frac{p}{\omega_0} + \frac{\omega_0}{p} \right)}$
Corresponding Frequencies			
$\frac{\omega_L}{\omega_c}$	$-\frac{\omega_0}{\omega}$	$\left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \frac{1}{2B}$	$\frac{-2B}{\left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)}$
Transfer Function First Order Model			
$\frac{1}{1 + \frac{p_L}{\omega_L}}$	$\frac{\frac{p}{\omega_0}}{1 + \frac{p}{\omega_0}}$	$\frac{2B_1 \frac{p}{\omega_0}}{1 + 2B_1 \frac{p}{\omega_0} + \left( \frac{p}{\omega_0} \right)^2}$	$\frac{1 + \left( \frac{p}{\omega_0} \right)^2}{1 + 2B_1 \frac{p}{\omega_0} + \left( \frac{p}{\omega_0} \right)^2}$
Second Order Model			
$\frac{1}{1 + 2\xi_L \frac{p_L}{\omega_L} + \left( \frac{p_L}{\omega_L} \right)^2}$	$\frac{\left( \frac{p}{\omega_0} \right)^2}{1 + 2\xi_L \frac{p}{\omega_0} + \left( \frac{p}{\omega_0} \right)^2}$	$\left[ \frac{2B_1 \left( \frac{p}{\alpha \omega_0} \right)}{1 + 2\xi \left( \frac{p}{\alpha \omega_0} \right) + \left( \frac{p}{\alpha \omega_0} \right)^2} \right] \left[ \frac{1 + \left( \frac{p}{\omega_0} \right)^2}{1 + 2\xi \left( \frac{p}{\alpha \omega_0} \right) + \left( \frac{p}{\alpha \omega_0} \right)^2} \right]$	$\left[ \frac{1 + \left( \frac{p}{\omega_0} \right)^2}{1 + 2\xi \left( \frac{p}{\alpha \omega_0} \right) + \left( \frac{p}{\alpha \omega_0} \right)^2} \right] \left[ \frac{1 + \left( \frac{p}{\omega_0} \right)^2}{1 + 2\xi \left( \frac{p}{\alpha \omega_0} \right) + \left( \frac{p}{\alpha \omega_0} \right)^2} \right]$
Definitions			
$\omega_c$ cut off frequency	$\omega_0' = \frac{\omega_c \omega_0}{\omega_L}$	$B_1 = B \frac{\omega_L}{\omega_c}$	$B_1 = B \frac{\omega_c}{\omega_L}$
$\omega_L$ natural frequency of 2nd order factor		$\xi = \frac{2\xi_L B_1}{\alpha + \frac{1}{\alpha}}$	
$\xi_L$ damping ratio		$\alpha = \sqrt{\frac{B_1^2 + 1 + \sqrt{B_1^2 + 2(1 - 2\xi_L^2)B_1^2 + 1}}{2}}$	
$p_L$ low pass Heaviside operator		$+ \sqrt{\frac{B_1^2 - 1 + \sqrt{B_1^2 + 2(1 - 2\xi_L^2)B_1^2 + 1}}{2}}$	
$\omega_L$ low pass radian frequency		$B = \frac{\omega_{CU}' - \omega_{CL}'}{2\omega_0}$	$= \sqrt{\omega_{CU} \omega_{CL}}$

Table b. LOW PASS TRANSFER FUNCTIONS

ORDER	BUTTERWORTH	PAYNTER
1.	$\frac{1}{\left( 1 + \frac{p}{\omega_c} \right)}$	
2.	$\frac{1}{\left( 1 + \sqrt{2} \frac{p}{\omega_c} + \left( \frac{p}{\omega_c} \right)^2 \right)}$	$\frac{1}{\left( 1 + 3 \frac{p}{\omega_c} + 4 \left( \frac{p}{\omega_c} \right)^2 \right)}$
3.	$\frac{1}{\left( 1 + \frac{p}{\omega_c} \right) \left( 1 + \frac{p}{\omega_c} + \left( \frac{p}{\omega_c} \right)^2 \right)}$	$\frac{1}{\left( 1 + 2 \frac{p}{\omega_c} \right) \left( 1 + 1.2 \left( \frac{p}{\omega_c} \right) + 1.6 \left( \frac{p}{\omega_c} \right)^2 \right)}$
	$\omega_c = 3 \text{ db frequency}$ $ A  = .7 \text{ when } \omega = \omega_c$ $ A ^2 = \frac{1}{1 + \left( \frac{\omega}{\omega_c} \right)^{2n}}$	$\phi_{180} \approx \pi \frac{\omega}{\omega_c}$

**3.28(c)**

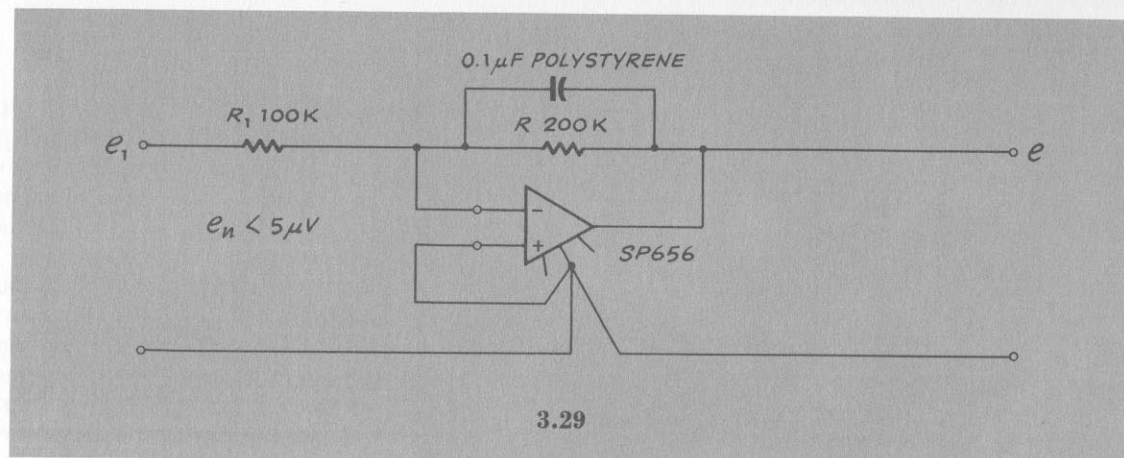
III.28  
II.1  
to  
II.4  
II.15  
to  
II.18  
III.22  
to  
III.27



**III.29 PRECISION DC AMPLIFIER.** A low-drift (i.e., chopper-stabilized) single-ended amplifier, carefully grounded to preserve a true “high-quality” ground point common to input, output, and power circuits, if deliberately limited in bandwidth to reduce effective noise and ensure stability by a low-leakage (Polystyrene) feedback capacitor, will provide an extremely precise (1PPM) DC amplifier exhibiting, typically, less than 5 microvolts of null uncertainty. Under those circumstances, for DC and low-frequency signals, we may write that:

$$-e = \frac{R}{R_1} e_1 \quad (3-11)$$

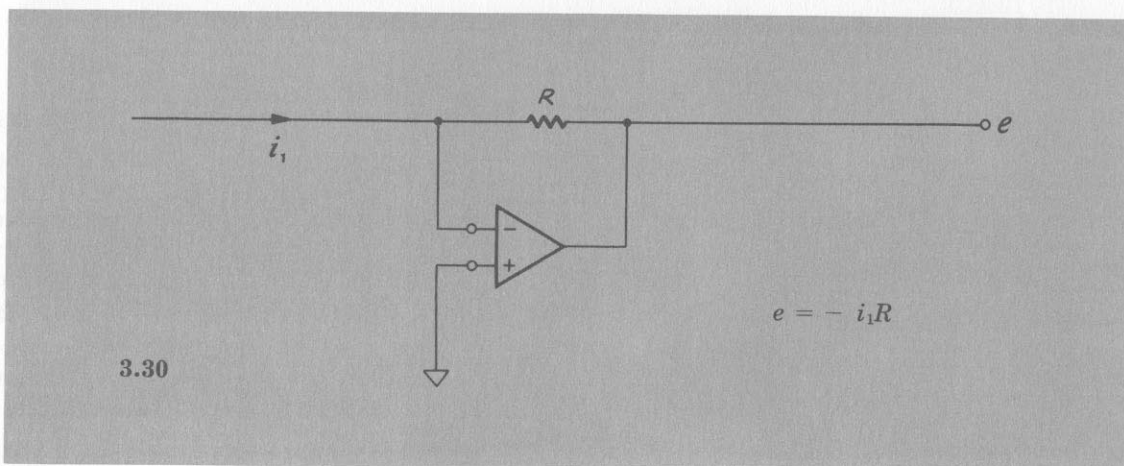
to an accuracy almost entirely dependent on the absolute accuracy of the input and feedback resistors themselves. (At  $e_1 = 5$  V, for example,  $e_n$  would be less than 1 PPM!)



III.29  
I.7  
to  
I.18  
II.1  
to  
II.4  
III.1  
III.2  
III.35  
III.36  
III.39  
III.42  
III.61

**III.30 CURRENT-TO-VOLTAGE TRANSDUCER.** In this simple powerful circuit, the output voltage is a direct function of the input current,  $e = -i_1 R$ . This “zero-drop” shunt provides an exceptionally inexpensive and convenient means of current measurement, since it not only introduces negligible voltage drop into the circuit, but its output voltage is developed at a low-impedance, high-energy level, capable of driving recorders, meter movements, or analog-to-digital converters.

For example, for  $10^{-7}$  amperes full scale,  $R = 10^7 \Omega$  yields a one-volt output with at least 2-milliampere capability.



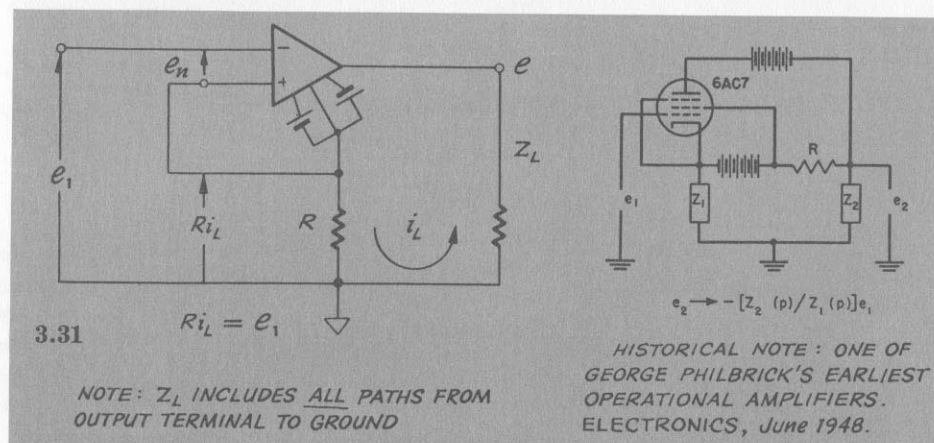
III.30  
II.1  
II.3  
II.4  
III.31  
III.36  
III.38  
III.40  
III.59  
III.60  
III.61  
III.79

**III.31 VOLTAGE-TO-CURRENT TRANSDUCER.** This circuit establishes and maintains a precise proportionality between  $e_1$ , the input voltage, and  $i_L$ , the output current, such that

$$i_L = \frac{e_1}{R} \quad (3-12)$$

The proportionality is *independent* of  $Z_L$ , within the limitations of amplifier output voltage ratings. This proportionality arises from the fact that, so long as  $e_n$  is negligibly small with respect to  $e_1$ , and the amplifier input current is negligible with respect to  $i_L$ , the output voltage will drive current through  $Z_L$  and  $R$  so as to make  $i_L R = e_1$ .

Note that the power supply “floats” with respect to signal ground. If the chassis ground (which is also the AC ground) is tied to the signal ground and if there is not good electrostatic isolation between the primary and secondary, an error current will be induced to flow between chassis ground and power common returning through the load and amplifier.



III.31  
II.1  
to  
II.4  
III.3  
to  
III.9  
III.30  
III.80

**III.32 SIMPLE FOLLOWER.** As described earlier, the simple voltage follower reproduces, to a very high accuracy, the input voltage  $e_1$ , without sign reversal—provided, of course, that  $e_n$  is very small compared to  $e_1$ . In the follower, the output is fed directly back to the negative input as degenerative feedback at high gain. Phase distortion and attenuation are negligible over the frequency range in which the amplifier gain is  $\gg 1$ . Input impedances from tens of megohms, to tens of gigohms and output impedances well below an ohm are easily obtained; as can be seen from the following expression, which relates input impedances to circuit and amplifier parameters, as shown in the circuit diagram:

$$Z_{in} = Z_{AG} * || (Z_n \times \text{loop gain}) \quad (3-13)$$

\*Ref. 1.18(c) ...  $Z_{AG} || Z_n \equiv \frac{Z_{AG} Z_n}{Z_{AG} + Z_n}$

**III.33 CHOPPER-STABILIZED FOLLOWER.** Back in I.12, we described chopper stabilization of an Operational Amplifier, noting that the circuit usually employed left us with a single-ended amplifier. Such an amplifier would not lend itself to use as a conventional follower, such as that shown in III.32; however, by using the connection shown here, with the normal output circuit grounded, and the power-supply common return used as the output terminal, follower behavior is achieved. The capacitance and leakage to ground of the power-supply common terminal

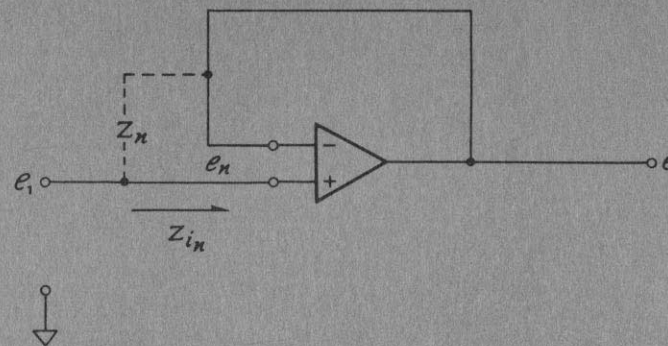
are, of course, loading the output, but the output impedance is low enough, at least at low frequencies, to tolerate such loading.

Chopper-stabilized followers generally have exceptionally low attenuation at or near “DC,” and very low drift. The input impedances are high at low frequencies, too. Typical values are: gain; 1.0000000 ( $\pm 0.1$  PPM attenuation at “DC”); input impedance:  $> 10^{12}$  ohms.

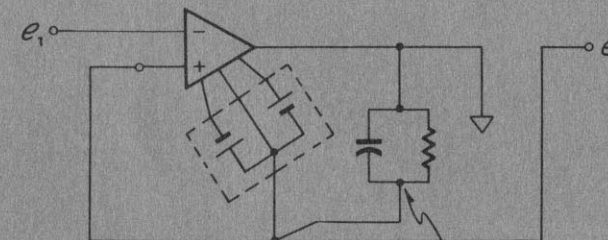
Note that this circuit is an inverted version of III.32.

**III.34 PRECISION HIGH-VOLTAGE FOLLOWER.** Combining the best of two worlds, this circuit makes use of the wide dynamic range of a vacuum-tube cathode-follower circuit, and the high gain of a solid-state Operational Amplifier to produce a precise follower with high voltage range capability. The power supply of the Operational Amplifier rides along with the output voltage  $e$ . Diode pairs protect the amplifier input, and back-to-back zeners protect its output, in the traditions established in I.27. A principal limitation will be imposed by the insulation of the amplifier and power supply from the ground; another is dynamic

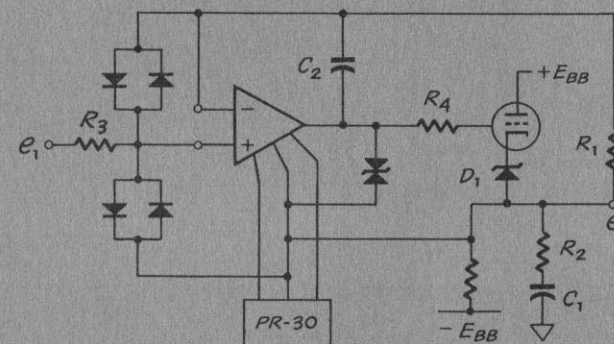
stability (the amplifier’s gain and the triode’s  $\mu$  are cascaded).  $R_2$ – $C_1$ ,  $C_2$ , and  $R_4$  are introduced to stabilize the circuit against RF parasitic oscillations.  $R_1$  and  $R_3$  are current limiters, and are not large enough in value, compared to the input impedances they precede, to affect gain.  $D_1$  establishes a convenient zero-signal (quiescent) bias level for the triode, and the Operational Amplifier output automatically seeks an appropriate quiescent level to satisfy the demands of the feedback around the circuit, while overcoming the contact-potential vagaries of the triode.



3.32



3.33



3.34

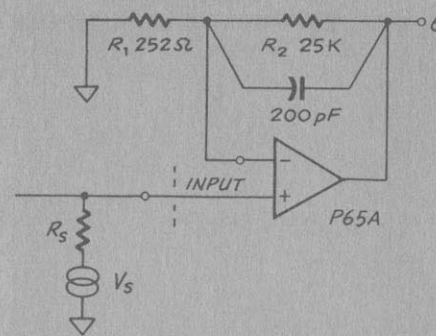
III.32  
I.22  
II.2  
III.33  
III.34

III.33  
I.7  
I.8  
I.9  
I.10  
I.11  
I.12  
I.13  
I.14  
I.18  
I.23  
II.2  
III.32  
III.34

III.34  
I.7  
I.8  
I.9  
I.10  
I.11  
I.12  
I.13  
I.14  
I.18  
I.23  
II.2  
III.32  
III.33



**III.35 LOW-NOISE PRECISION PRE-AMPLIFIER.** In this application of a follower with gain (see II.2) a precise gain of 100 is achieved, using moderately low impedances for optimum response and signal-to-noise ratio. Very precise, low-noise performance can be obtained with low impedance sources such as thermopiles or bridge circuits, as the data in figure 3.35 spell out. For source impedances of 10 to 100 k $\Omega$ , very good noise figures can be obtained (3 to 6 db, typically). The amplifier noted will perform very well, but for optimum noise figure an amplifier with field-effect transistors (i.e., model P25A) is recommended.



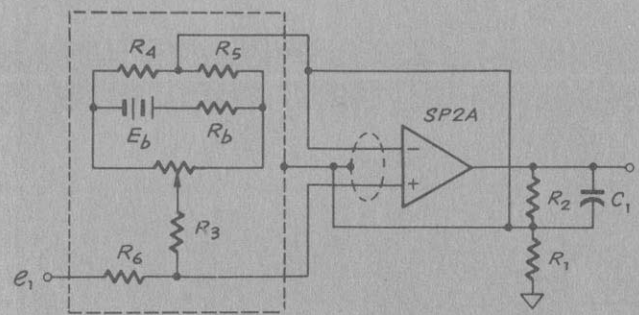
3.35

**TYPICAL PERFORMANCE**  
 DC Gain = 100.0  
 Bandwidth = 25 kHz (3 db down)  
 Linearity = 0.1% or better  
 Output Impedance < 20 $\Omega$  below 1 kHz  
 Voltage Noise: 1.1  $\mu$ V RMS (160 Hz–16 kHz)  
 (Referred to input, for  $R_s \leq 1$  k $\Omega$ ) 2.0  $\mu$ V RMS ( $\frac{1}{4}$  Hz–25 kHz)  
 Noise Figure  
 ( $R_s = 20$  k $\Omega$ ): 5 db ( $\frac{1}{4}$  Hz–25 kHz)  
 Input Impedance: 50 M $\Omega$  || 6 pF  
 Long-Term Drift: 50  $\mu$ V per week or better at constant temperature

**III.36 SOLID STATE ELECTROMETER.** The low-noise circuit just discussed in III.35 may be suited to electrometer service by adding the circuit modifications shown here:

- $E_b$ ,  $R_3$ ,  $R_4$ , and  $R_5$  make up a reversible current-offset-biasing circuit “bootstrapped” to extremely high impedance compared to  $R_6$ , so that the gain loss is negligible.
- $C_1$  is made large enough to narrow the bandwidth to a few cps, for lowest “white-noise” effect.
- $R_b$  is chosen for optimum current bias sensitivity.
- Guarding of the input lead is provided, and returned to the negative input terminal.

Typical circuit values and performance are shown. For best performance, this circuit is not recommended for applications in which the operating temperature exceeds 50°C, and the lower the temperature, the lower the offset current and current noise.



3.36

$$e = \left(1 + \frac{R_2}{R_1}\right) e_1$$
  
 $E_b = 1.3$  V  
 (Pot) || ( $R_4 + R_5$ ) = 100 k $\Omega$   
 $\Delta E = \pm 6.5$  mV  
 For  $\Delta I = \pm 2 \times 10^{-12}$  A  

$$R_3 = \frac{\Delta E}{\Delta I} = \frac{6.5 \times 10^{-3}}{2 \times 10^{-12}} \cong 3$$
 kM $\Omega$   
 $R_6 = 10$  M $\Omega$  (protects  $e_1$  source against faults)

**III.37 NEUTRALIZING INPUT CAPACITANCE.** In circuits employing the follower-with-gain configuration, the effects of capacitance to ground at the input terminal, whether due to input-cable shielding, strays, or amplifier input shunt capacitance, or any combination of the three, may be neutralized almost perfectly by connecting a capacitor,  $C_n$ , as a regenerative-feedback path from output to input, as shown here.

The undesired shunt input capacitance,  $C_s$  draws a current:

$$i_s = C_s p e_A \quad (3-14)$$

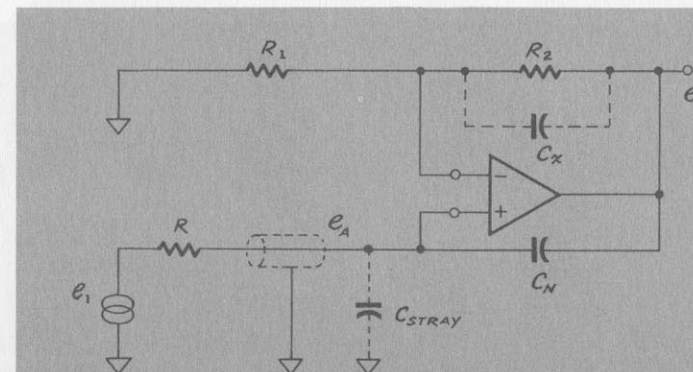
For perfect neutralization,  $C_n$  should draw an equal but opposite current:

$$i_n = C_n p (e - e_A) = i_s = C_s p e_A \quad (3-15)$$

Thus  $C_n$  should be selected so that, for  $e_n$  negligible compared to  $e_1$ ,

$$C_n = C_s \left( \frac{R_1}{R_2} \right) \quad (3-16)$$

If  $C_n$  is too large, oscillation could occur, but  $C_x$  will prevent that. Note that much the same scheme may be used to “neutralize” leakage and other shunt input resistances, but the value of the neutralizing resistor becomes so large that a Tee network (see I.26) may be necessary.



3.37

III.35  
 I.7  
 to  
 I.18  
 I.50  
 II.2  
 III.36  
 III.42  
 III.61

III.36  
 I.7  
 to  
 I.18  
 I.34  
 I.49  
 I.50  
 II.1  
 to  
 II.4  
 III.29  
 III.35  
 III.38  
 III.42  
 III.61

III.37  
 III.71  
 III.72

**III.38 LOW-NOISE PRECISION CURRENT AMPLIFIER.** This is the circuit of choice when the input current is referenced to ground and the load is floating. (If the load may not float, a circuit such as 3.7 must be used.)

In this rather more complex version of the current-to-voltage transducer of III.30, the current through the load,  $Z_L$ , is monitored by a low-resistance shunt,  $R_s$ , after which that signal  $e_s$  is fed back through a Tee network (see I.26) made up of  $R_3$ ,  $R_2$ , and  $R_1$ , to the summing point, which is at a virtual ground. The load may be complex and active, within the limitations of the output voltage rating of the booster, but it must be amenable to “floating” off ground by  $e_s$  and  $R_s$ . With high-performance amplifier (such as either of those noted) the DC current gain of this circuit is given by:

$$\frac{i_L}{i_{in}} = \left( \frac{R_1}{R_s} \right) \left( 1 + \frac{R_3}{R_2} \right) \quad (3-17)$$

For dynamic stability, feedback capacitance  $C_1$  or  $C_2$  (or both) is usually in order.

### III.39 VERY-HIGH-IMPEDANCE DIFFERENTIAL INPUT AMPLIFIER.

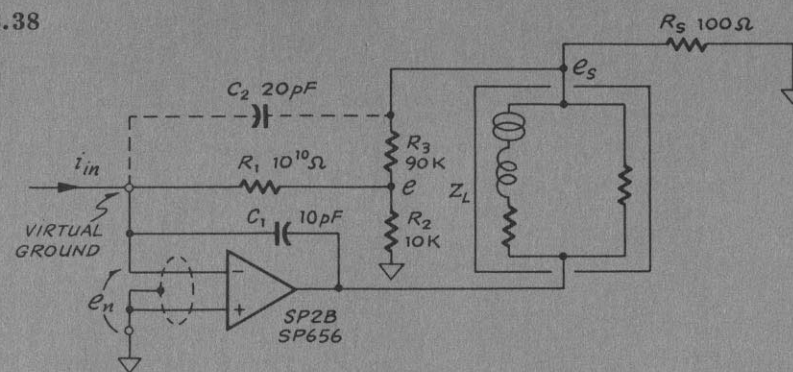
This circuit combines the low output impedance of a symmetrical subtractor (see II.5) and the very high input impedance and  $CMRR$  of a dual-amplifier balanced differential input stage. The output stage is straightforward, and requires no special comment other than the observation that, since the circuit is being driven from the low impedance outputs of the dual-differential-stage amplifiers, the impedance levels of the feedback and divider networks in the subtractor may be kept quite low, for good stability and bandwidth. The input stage is interesting in that (unlike a pair of followers-with-gain, which magnify both common-mode and differential signals) this cross-coupled circuit passes the common-mode signal at *unity gain*, but amplifies the differential signal with a gain of  $(1 + m + n)$ .

The limit of common-mode error is established by the degree to which the error voltages,  $e_n$ , for the two amplifiers: (a) approach zero, and (b) track one another.

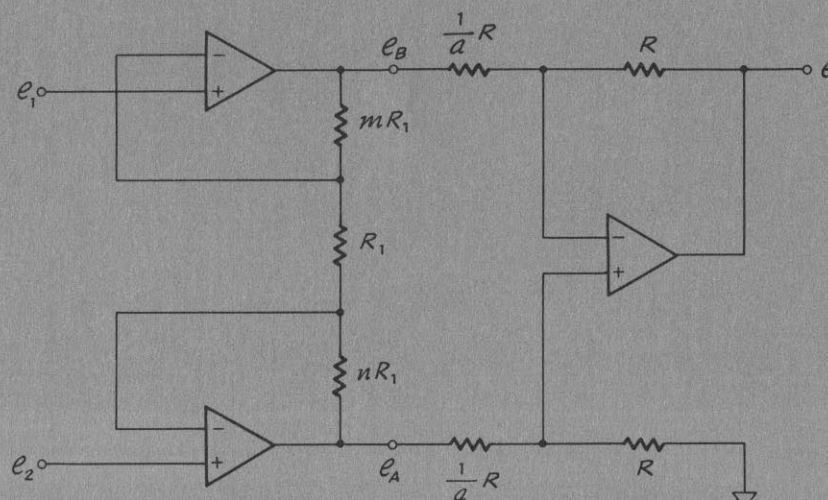
The input impedances—both common-mode and differential—are extremely high, as might be expected of follower configurations, so that the circuit is almost completely insensitive to unbalances in source impedance of  $e_1$  and  $e_2$ , and the input terminals are very close to “passive”—i.e., there is negligible interaction between the input terminals.

This circuit, equipped with the recommended amplifiers, constitutes an extremely high-performance differential-to-single-ended transition, with excellent gain, bandwidth and stability. It may be supplemented, of course, with a booster, if need be.

3.38



III.38  
I.7  
to  
I.18  
I.34  
I.49  
I.50



$$e = a(1 + m + n)(e_2 - e_1)$$

BEST PERFORMANCE  
P25A's  
SP2A's  
LOWEST COST  
EP55AU's

BEST PERFORMANCE  
P85A  
P35A  
LOWEST COST  
EP55AU

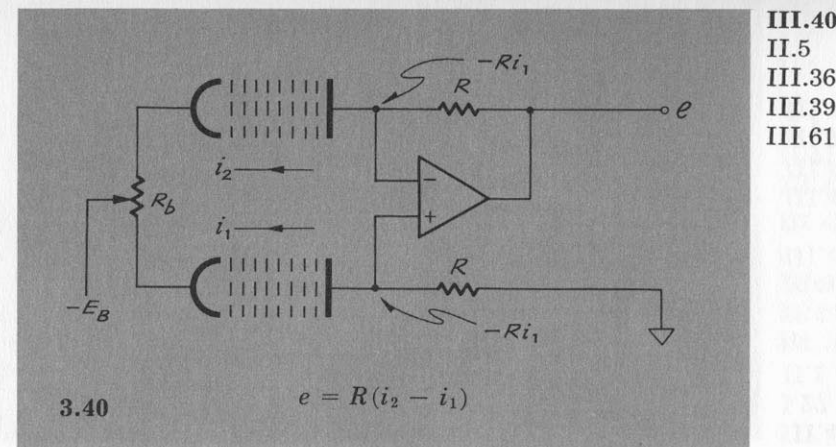
3.39

III.39  
I.7  
I.8  
I.9  
I.10  
I.11  
I.12  
I.13  
I.14  
I.15  
I.16  
I.18  
I.48  
II.1  
II.2  
II.3  
II.4  
II.5



**III.40 PHOTOMULTIPLIER-DIFFERENTIAL CURRENT AMPLIFIER.** The Adder-Subtractor is very well suited to the conversion of the difference between small currents to a husky voltage at manageably-low impedance levels. In this example, the small currents are supplied by photomultiplier tubes operated from a power supply of hundreds to thousands of volts. The response of this circuit is linearly and accurately proportional to the difference between the two photomultiplier currents. Since the feedback networks cannot have more than about 10 volts across them, and probably

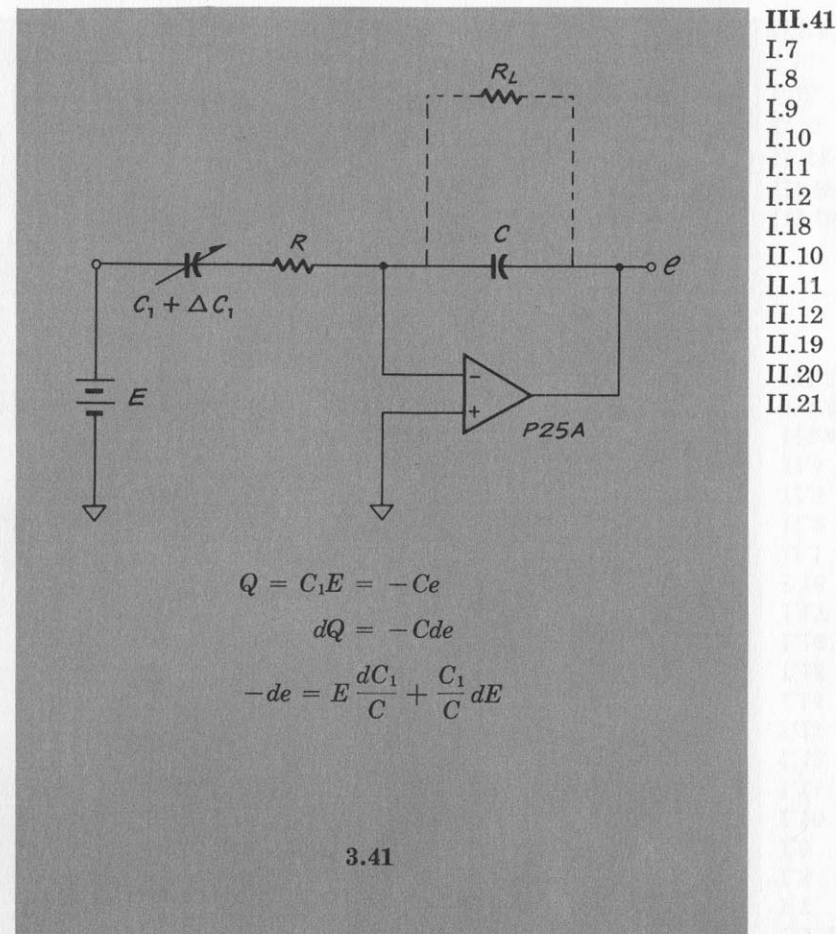
have less than 5, the amplifier end of the circuit operates comfortably near ground, compared to  $-E_B$ ; thus, the ultor voltages cannot vary by any large percentage with the current through them, so that the sensitivity will remain relatively constant, even with sizeable current differences.  $R_B$  is a zeroing control, and is meant to provide "dark-current" balancing. It may be used to set an *arbitrary* zero level at any standard level of light intensity. Typically, with  $R = 10^8$  ohms, this circuit will drive a 1,000-ohm, 1 mA recorder full-scale for a current difference of only 10 nanoamperes.



**III.41 CHARGE AMPLIFIER.** Capacitive transducers are often employed to accomplish the conversion of some mechanical, thermal, chemical, etc. phenomenon to electrical information. They respond to physical stimuli by providing varying electrical charge, which can often be considered as a constant voltage source in series with a variable capacitor, or vice versa. Typical of these is the capacitance microphone, represented in our drawing as a battery,  $E$ , in series with a capacitance  $C_1 + \Delta C_1$ . An Operational Amplifier, connected as shown, provides an ideal transition from change of capacitance to change of output voltage . . . unloading, linearizing, and providing appreciable output current and voltage capabilities.

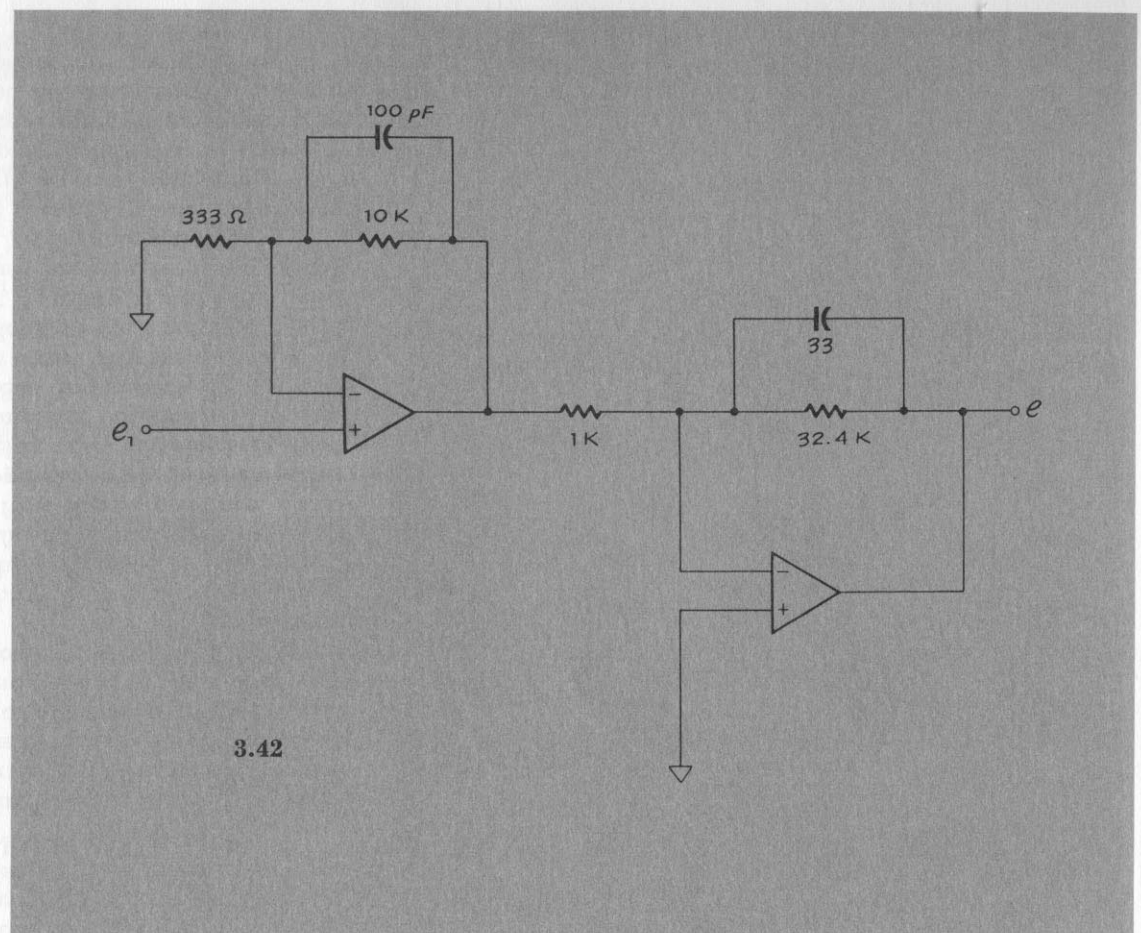
output. Compare this circuit with that of the current-to-voltage transducer of III.30: resistors convert current to voltage; capacitors convert charge to voltage.

Note that this circuit has the desirable property of being virtually independent of shunt capacitance across the input, since such capacitance is connected from the summing point to ground, and has across it only the residual null voltage, which should be negligibly low in practical application. This independence of input capacitance permits the use of long shielded cables between the transducer and the amplifier, without significantly affecting the accuracy of the conversion from charge to voltage. Leakage resistance in parallel with  $C$ , on the other hand, must be deliberately sustained, in order to prevent the amplifier output from drifting to saturation. (See Integrators, particularly II.12.) It will be noted that the sensitivity is inversely proportional to the value of the feedback capacitance; therefore, the smallest value that will be large compared to "strays" will yield the highest predictable sensitivity. One must then be sure that at the lowest frequency of interest,  $X_C$  will be small compared to  $R_L$ , and that the amplifier's offset current will be sufficiently small to prevent saturation with the required value of  $R$ . Amplifiers employing field-effect transistors are recommended for this application.



**III.42 WIDE BAND, GAIN-OF-1000 AMPLIFIER.** The wide bandwidth of this circuit is the result of cascading two amplifiers, producing a resultant gain-bandwidth which is about half the product of the two. It generally makes good sense to use the same amplifier type in both positions—however, if that is not done, for other reasons, the gain required of each stage should be directly proportional to the gain-bandwidth product of the amplifier associated with that stage, for optimum resultant bandwidth.

The circuit consists of a follower with gain (see II.2), appropriately rolled off for stability by means of a suitable feedback compensating capacitor, driving an inverting stage with gain, similarly compensated against instability. If the wiring is carefully done so as to minimize strays, the necessary roll-off capacitor should not significantly limit the bandwidth, particularly if the impedance levels are held to minimum, as shown. An outstanding advantage of this circuit is the fact that though low impedances are used in the feedback groups, the follower configuration used for the first stage provides very high input impedance, and the second stage is driven by the relatively low output impedance of the follower, and exhibits a reasonably low output impedance itself. Thus, with a total of only 6 external components, and 2 economical, standard amplifiers, we have constructed a precise, stable, low-noise, wideband (about 50 kHz) amplifier with a gain of 1000. Note that the amplifier response extends all the way down to DC, and that the noise and uncertainty levels, referred to the input, are of the order of microvolts, using the recommended amplifiers. This circuit will find wide use in instrumentation and computation circuits, and its utility can be further extended by the addition of a booster stage, when necessary.

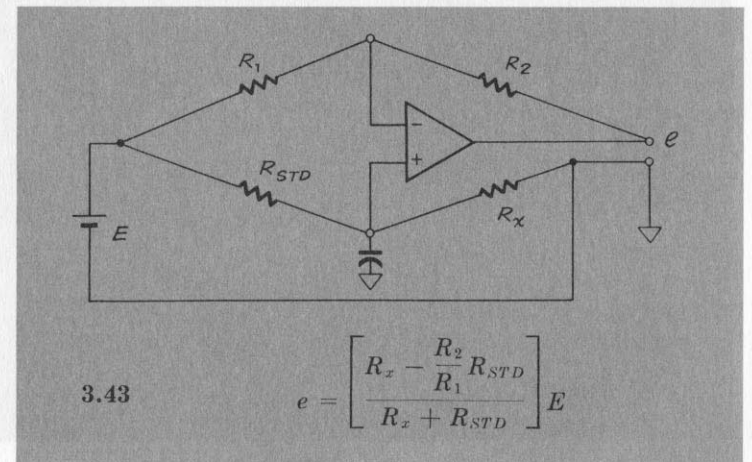


3.42

### III.43 WHEATSTONE BRIDGE—DEVIATION MEASUREMENT CIRCUIT.

This application of the basic Adder-Subtractor circuit (II.5) has many advantages over a conventional Wheatstone bridge or deviation-bridge circuit. In this configuration, the bridge excitation voltage  $E$  is applied as a signal to both the Adder and the Subtractor networks, and the amplifier output voltage indicates the extent to which  $R_1/R_2$  does not conform to  $R_{STD}/R_x$ . Note the following advantages: (1) The unknown,  $R_x$ , is grounded, which aids in guarding and shielding; (2) Provided that  $e$  does not saturate when  $R_x$  is removed or shorted, there is always some value of  $E$  within the linear region that will “balance” the bridge

under those extreme conditions; (3) It is perfectly practical to drive very large current through  $R_x$  since only  $R_{STD}$  is involved in that path, but none of the instrument circuitry need carry those currents; (4) The read-out is grounded, which is a very considerable advantage if a sensitive or high impedance detector is to be used. (5) Unfortunately, the output  $e$  is linear only with  $R_2$ ; hence a linear calibration can be achieved only if the unknown is placed in the  $R_2$  instead of the  $R_x$  position, sacrificing some of the advantages previously mentioned. Note the use of a bypass capacitor across  $R_x$ , reducing the chance of stray coupling or pick-up.



3.43

$$e = \left[ \frac{R_x - \frac{R_2}{R_1} R_{STD}}{R_x + R_{STD}} \right] E$$

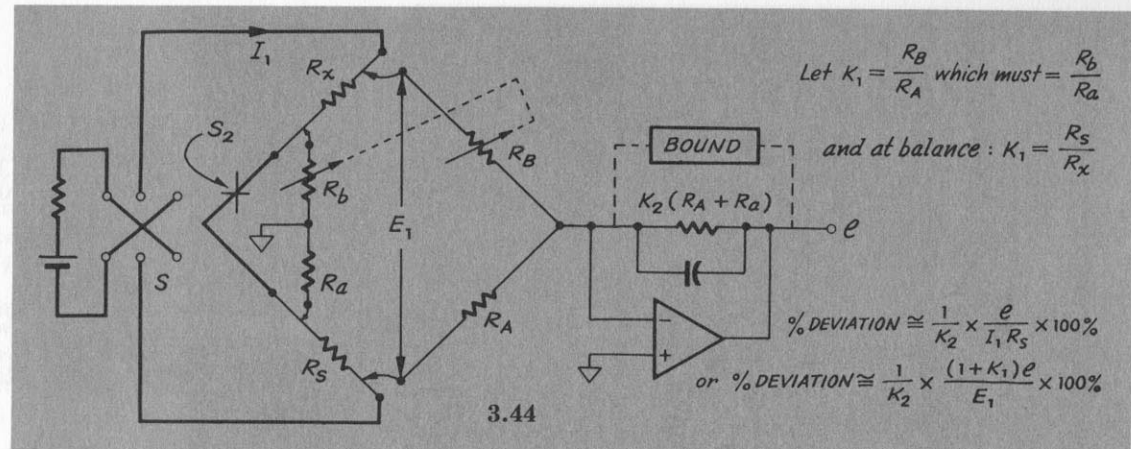
III.42  
I.7  
I.8  
I.9  
I.10  
I.11  
I.12  
I.13  
I.14  
I.15  
I.16  
I.17  
I.18  
II.1  
II.2  
II.3  
II.4  
III.35  
III.36  
III.38

III.43  
I.27  
II.1  
to  
II.4  
II.41  
III.44  
to  
III.48  
III.58  
III.78  
III.79



### III.44 KELVIN-DOUBLE-BRIDGE DEVIATION INDICATOR (EXCITATION FLOATING).

A current-to-voltage transducer circuit (à la III.30) makes a very effective detector and linear deviation indicator for a Kelvin Double Bridge used for low-resistance (e.g., sub-ohm) measurements, provided that the DC bridge excitation source may float. The unknown four-terminal resistance,  $R_x$ , is measured by comparing it with a fixed or variable standard,  $R_s$ , of the same order of magnitude, with the switch closed.  $R_a$  and  $R_b$  compensate for lead and contact resistance, provided that they are precisely proportional to  $R_A$  and  $R_B$ . This proportion is proved if the bridge is balanced with switch  $S$  open.

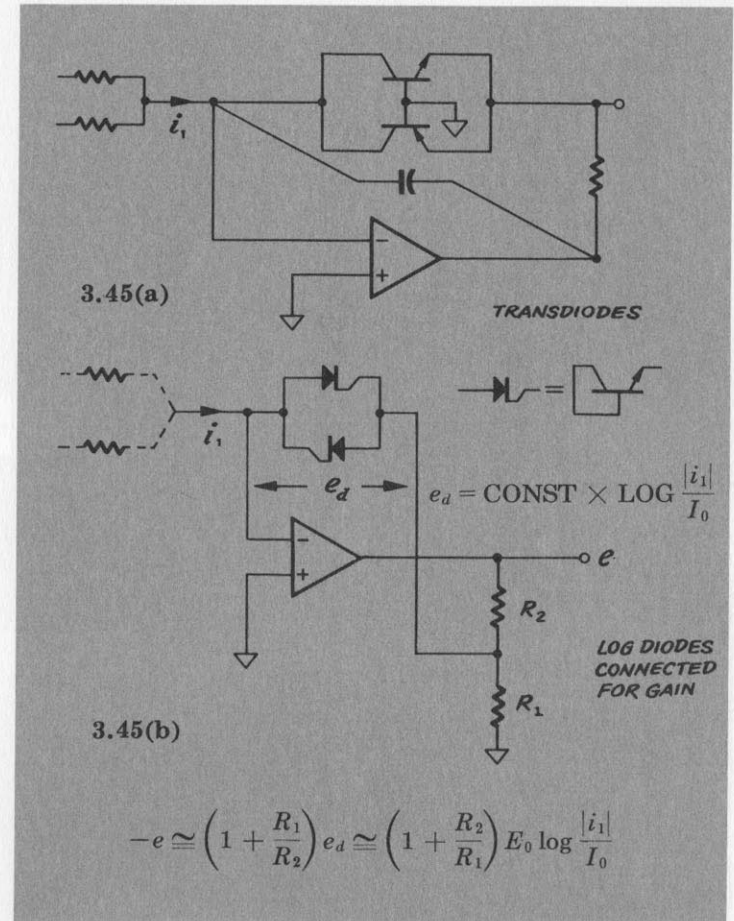


### III.45 SIMPLE LOGARITHMIC-RESPONSE NULL-DEVIATION AMPLIFIER.

The current-to-voltage transducer of III.30 makes an excellent null detector, because of its high current sensitivity and low voltage drop, as noted earlier. In many applications, however, this high sensitivity may be a mixed blessing, because null detectors must often function in circuits that can and do operate "off-null" for long periods of time, causing saturation (or requiring bounding) and giving little or no indication, when driven to saturation or bounding, of just how far off null they are—thus rendering adjustment of the external circuit difficult, and "touchy," even near null. One cure for this situation is the modification of the response characteristic to a predictable logarithmic characteristic. The circuit shown here takes advantage of the inherently logarithmic voltage-current characteristic of transistors connected as diodes (see II.22, or the Technical Data Sheet on Model PL1 Logarithmic Transconductor) to achieve a response in which the output is proportional to the logarithm of the input current, as shown on the drawing. The output voltage is fed back through back-to-back transdiodes to the summing point. (It should be noted that the diode

that is conducting, forms a bound circuit, such as that described in I.25.) The feedback circuit is so proportioned as to operate the diodes at currents in the range from less than  $10^{-8}$  to  $10^{-3}$  amperes, in which region their voltage/current characteristic most closely approaches a logarithmic relationship. For a given input current, then, the voltage drop across the diode will be  $E_0 \log (i/I_0)$  (since the diode current must equal the input current in the ideal case). Thus the output voltage is also proportional to the logarithm of the input current. The divider shown in (b) but equally applicable to (a) produces closed-loop gain; in the degenerate case, in which  $R_2 = 0$ , the output voltage is simply equal to the forward voltage of the conducting diode. The response equation shown on the drawing is based upon the above assumptions, as well as the usual "ideal case"—negligible amplifier input current and null voltage at the summing point, infinite gain, constant temperature, etc.

Adding a resistor across the diodes modifies the effective diode characteristic at very low currents, limiting the maximum sensitivity, if desirable.

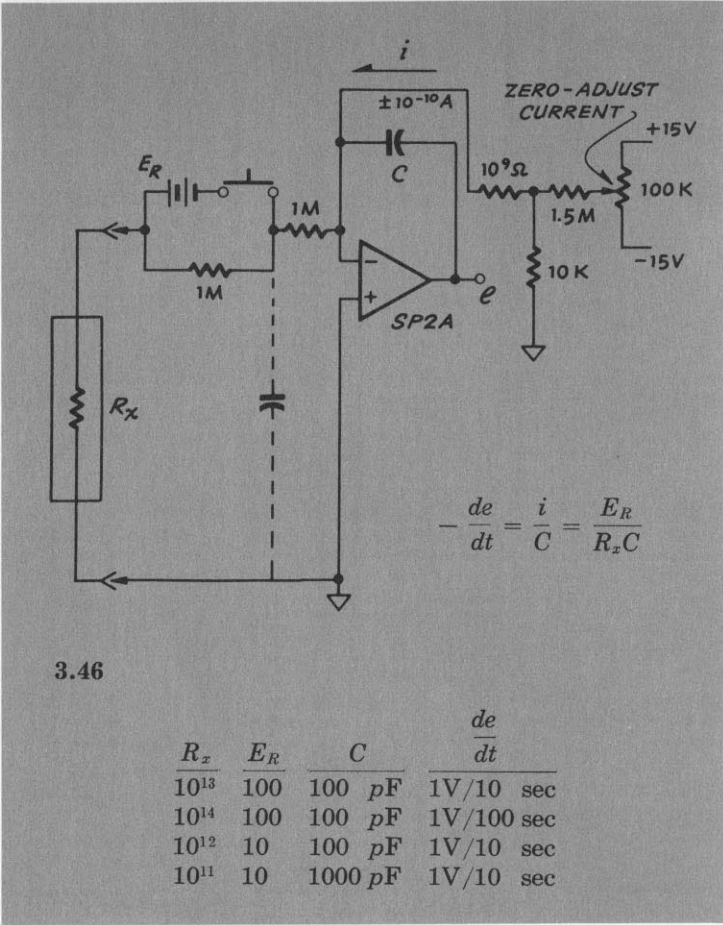


**III.46 INSULATION RESISTANCE, TERA-OHMS TO GROUND.** This application of an integrator has far-ranging implications to the instrument circuit designer, being but one of many examples of the use of charging time to measure small currents. In this application,  $R_x$  is an extremely high resistance—of the order of teraohms (1 teraohm =  $10^{12} \Omega$ ), measured between some test point and ground. After taking the usual precautions to prevent anomalous results—shielding, guarding and cleaning the resistance path in question—the circuit is connected to  $R_x$ , as shown, and the zero adjustment potentiometer is manipulated until there is no significant observable change in the output voltage with time. This condition reassures us that the net current into the integrator, including all of the usual pestilences—amplifier offset current, capacitor leakage, stray leakage, currents generated by thermal EMF's, etc.—is zero.

If we now close the push-button switch in series with  $E_R$ , an input current will flow that is almost exactly equal to  $E_R/R_x$ . (One may ignore the piddling megohm in series with the integrator input, compared to teraohms, of course.) This current will cause the output voltage to change at a rate determined by  $R_x$  and  $C$ , for a given value of  $E_R$ . Typical values

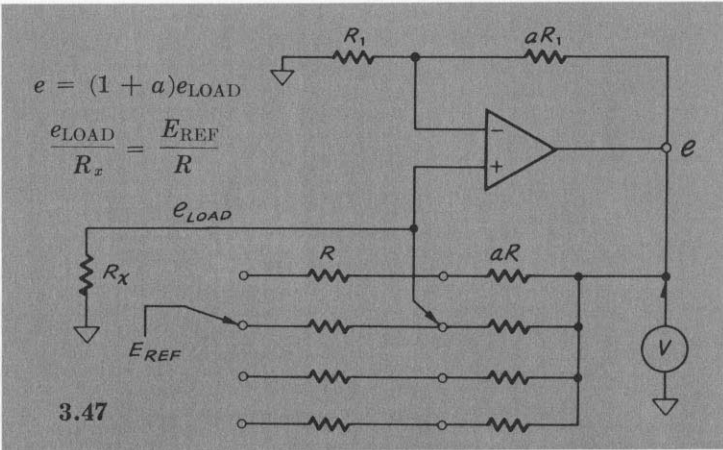
are shown in the chart appended to the drawing. For nominal accuracies, a stop watch and a conventional meter are adequate, since the test may be allowed to run for a time corresponding to 10 volts before the amplifier saturates. The circuit is capable of much higher accuracy, however, and the inventive reader will no doubt be tempted to automate the procedure, using a relay for the pushbutton, a comparator to detect the exact moment at which the output arrives at a critical value, and an accurate time-interval meter to record the elapsed time.

Note the suggested use of a modest bypass capacitor across the integrator input, to reduce the effects of pick-up. Note also the use of the Tee network into the zeroing circuit to reduce the value of the series resistor to a practical  $10^9$  ohms. This will tend to increase the noise gain for voltage errors at the summing point. However, as long as  $E_R$  is of the order of volts (compared to sub-millivolts), the gigaohm shunt load at the amplifier input will not be significant. Remember that the accuracy of the measurement is directly affected by the absolute accuracy to which  $E_R$  is known and maintained, and by the amplifier's current offset drift.



**III.47 RESISTANCE MEASUREMENT, GROUNDED SAMPLE.** For precise resistance measurements at relatively low voltage, over a very wide range of resistances, this interesting application of the Howland circuit is highly recommended. Note that range switching is accomplished by selecting resistance-ratio sets, the accuracy of which is always easier to establish and maintain than that of individual "standard" resistors. The same is true for the

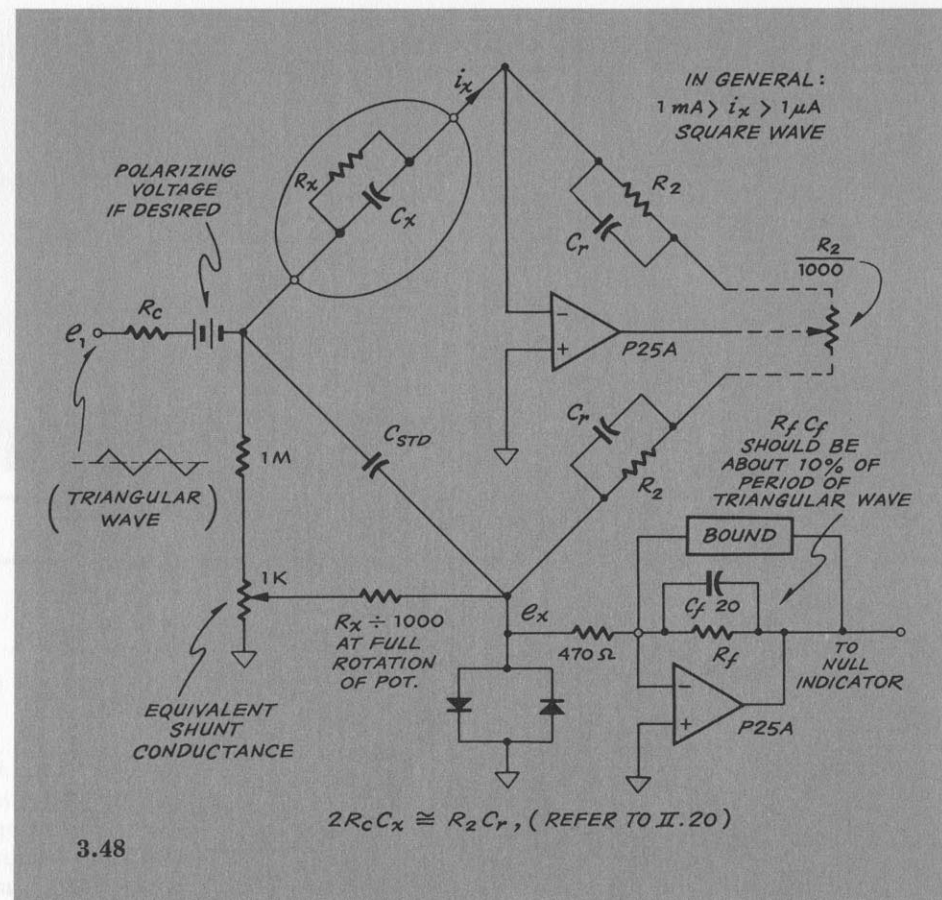
ratio set  $R_1/aR_1$ . Even wider ranges may be obtained by simultaneously switching the reference voltage . . . in decade steps, perhaps. Note that the ratio of the voltage across the sample to the output voltage is the divider ratio,  $a$ . If  $a$  is set to 100, for example, 10 millivolts across the sample will correspond to a 1 volt output, thus avoiding consideration of self-heating in all but the lowest resistance ranges.





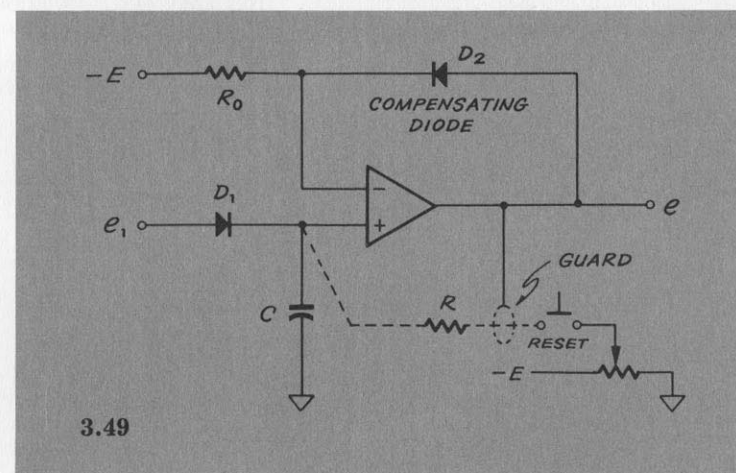
**III.48 PRECISE CAPACITANCE-DEVIATION BRIDGE.** There is no shortage of extremely precise capacitor bridges available to-day, but typically they use small voltage signals at relatively high frequency. This intentionally excludes such effects as voltage coefficient and polarization. Furthermore, the effects of shunt (leakage) resistance, series resistance; dielectric and other losses are lumped together in most bridges as the "dissipation factor," while the series inductance tends to lower the indicated capacitance somewhat. For measuring capacitors to be used in analog integrating circuits, there is no substitute for operating them under conditions similar to the anticipated use, e.g. driving ("integrating") them slowly over the voltage range (as shown here) with a constant current of perhaps 1 to 1000 microamperes, again selected to simulate the intended service.

The excitation,  $e_1$ , applied to this bridge should be a triangular wave for maximum resolution (although a sine wave can serve well). A triangular wave provides approximately constant current, first positive, then negative. Thus the output of the amplifier is a fair square wave of voltage, and the null error voltage will be a small square wave (of sorts) for a small mismatch between the unknown capacitance and the standard. Tilt in the square wave implies a difference in shunt leakage, whereas a "bow" implies a difference in voltage coefficient between the unknown and the standard. Series resistance or inductance of the amounts found in practical capacitors for precision integrators will not affect the balance; neither, in general, will the shunt (leakage) conductance. The potentiometer,  $R_2/1000$ , can be used when a readout of the percentage deviation is desired, the extremes of the potentiometer representing about  $\pm 0.1\%$  difference between  $C_x$  and  $C_{std}$ .



**III.49 SIMPLE PEAK-READER AND MEMORY.** This circuit may be set to any of a wide range of initial conditions (i.e., the stored charge on  $C$ ), by adjusting the potentiometer. After reset, signals larger than the stored value will charge the capacitor, as rapidly as the source impedance permits. The capacitor will "remember" the most positive (or least negative) signal. The follower unloads the capacitor, provides unity gain, and low output impedance. If the diode is reversed, the circuit will remember the most negative signal applied to the input. Departures from the Ideal include: (1) reverse leakage in  $D_1$ , whenever the signal is at a lower value than the peak value

stored; (2) leakage (inherent in and stray) across the capacitor itself, as well as dielectric soakage; (3) amplifier input admittance and leakage current; (4) amplifier common-mode error; and (5) the forward drop (about 0.2 V) and effective source resistance of  $D_1$ —the first causing a gradually-decreasing magnitude error; the second slowing down the rate of decrease, primarily because of the increase in charging-time-constant, at low diode-drop.  $R$  limits the discharge current. Diode  $D_2$  provides first-order compensation for the average drop across  $D_1$ . Choose  $R_0$  and  $E$  for zero net offset error for the most probable amplitude and duration of peaks.



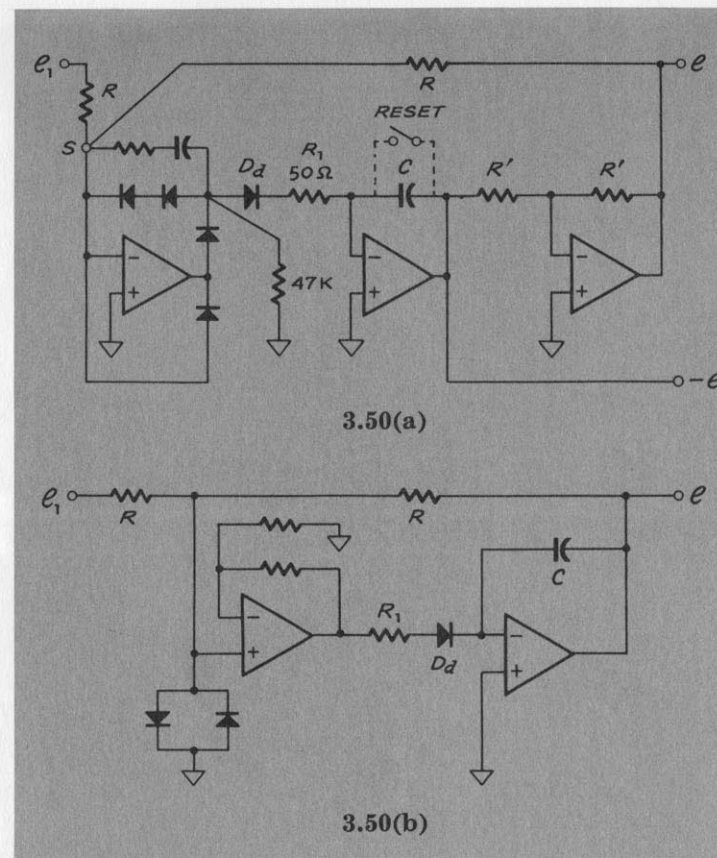
III.48  
I.7  
to  
I.18  
I.33  
II.10  
II.11  
II.12  
II.41  
III.43  
to  
III.46  
III.58  
III.78

III.49  
I.32  
I.33  
I.34  
II.1  
II.2  
II.3  
II.46  
II.47  
II.48  
III.50  
to  
III.53  
III.74  
III.75  
III.76

**III.50 PRECISION PEAK-READER & MEMORY.** This circuit can be broken down into a combination of three familiar elements: a precision electronic switch, of the type described in II.40, a track-and-hold memory (fast-charge integrator) of the type discussed in II.46, and the very familiar unity-gain inverter. The only new element introduced by this circuit configuration is the fact that all three of the circuits we have just enumerated are connected in a closed-loop configuration, with equal resistors ( $R$ ) to form a unity-gain inverter with peak reading and peak holding characteristics. As the circuit is shown, it follows only negative peaks, but, by reversing all of the diodes in the switch, including  $D_d$ , the decoupling diode, it can be made to follow positive peaks. The circuit performs as follows: negative-going value of  $e_1$  cause positive current rapidly to charge the integrating capacitor  $C$  (provided that  $R_1C$  is short compared to the fastest rate of change of  $e_1$ ) until the positive output of the inverter following the integrator corresponds to the largest negative peak of  $e_1$  (since the re-set switch was last

operated), at which time the error voltage at summing point  $S$  goes to zero, and diode  $D_d$  is rendered non-conducting. The unity-gain inverter acts as a buffer on the integrator output, and also provides the necessary polarity reversal, so that the *major* unity-gain inverter (from  $e_1$  to  $e$ , through  $R$  and  $R$ ) will function correctly. When  $e_1$  departs the peak value and becomes more positive—in circuit (a)—the precision switch remains open, and the integrator is prevented from discharging back through the switch by  $D_d$ . (The usual problems demand attention—leakage in  $C$ , input current in the integrator amplifier, closed-loop dynamic stability, and stray leakage.) Leakage in the decoupling diode is unimportant because the amplifier driving it will be observed to be the “perfect” halfwave rectifier whose output is zero for positive input. Assuming correct circuit design and most particularly, correct amplifier selection, this circuit will hold its peak for a period limited only by the capacitor’s leakage.

A two-amplifier alternative is shown in (b).



**III.51 SIMPLE PEAK-TO-PEAK READER.** Positive values of  $e_1$  charge  $C_1$  through  $D_1$ , and are remembered. Negative voltage peaks charge  $C_2$  through  $D_2$ , and are held there. Follower B input is then at the highest peak since  $C_1$  was reset, and follower A output is at the deepest valley since  $C_2$  was reset. The subtractor output is:

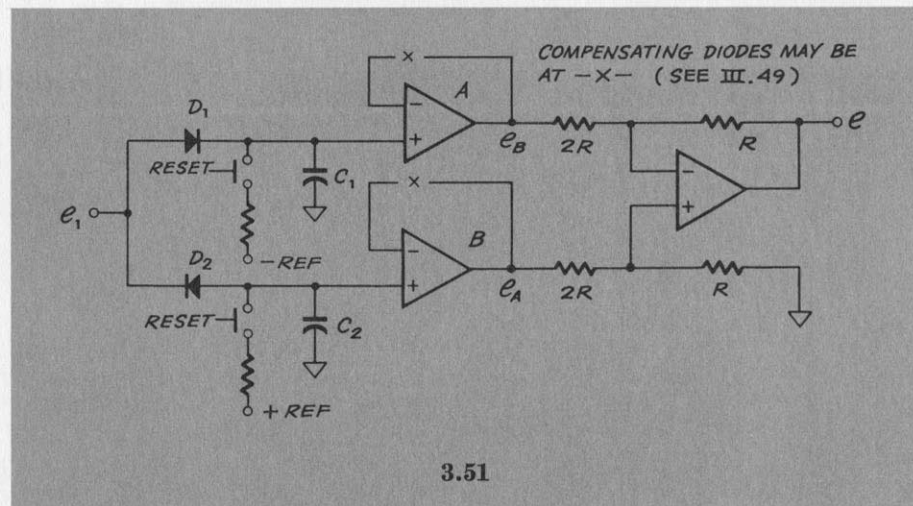
$$e = \frac{1}{2}(e_A - e_B) = -\frac{1}{2}(e_1 \text{ peak-to-peak}) \quad (3-21)$$

Reversing the input connections of the subtractor will yield

$$e = \frac{1}{2}(e_B - e_A) = +\frac{1}{2}(e_1 \text{ peak-to-peak}) \quad (3-22)$$

Diode and leakage errors prevent our calling this a precision device, but it has adequate accuracy for many purposes.

By closing the reset switches,  $e_B$  can be restored to the least value of  $e_1$ , and  $e_A$  to the maximum value of  $e_1$ , after which  $e_A$  and  $e_B$  may be driven by  $e_1$  to the fullest range of values within the circuit ratings.



III.50  
I.32  
I.33  
I.34  
II.1  
II.2  
II.3  
II.36  
II.37  
II.38  
II.39  
II.40  
II.46  
II.47  
III.49  
III.51  
III.52  
III.53  
III.74

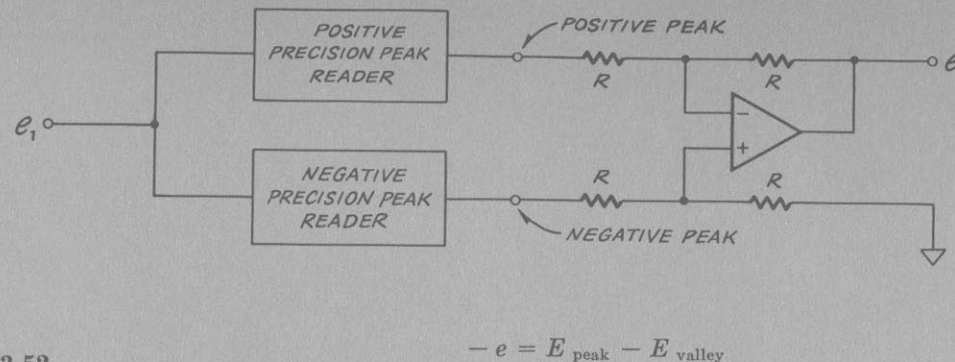
III.51  
I.32  
I.33  
I.34  
II.1  
II.2  
II.3  
II.36  
to  
II.40  
II.46  
II.47  
III.49  
III.50  
III.52  
III.53  
III.74



### III.52 PRECISION PEAK-TO-PEAK READER-MEMORY.

By combining two of the Precision Peak-Reader circuits described in III.50 and designing them with complementary diode polarities, so that one responds to and holds the highest positive peak, and the other the deepest "valley," and by combining these signals in a symmetrical Adder-Subtractor of unity-gain, we obtain an output equal to minus the maximum peak to peak amplitude, without reference to when the peaks occurred. Note that it is not absolutely necessary to use the Adder-Subtractor circuit—a voltmeter connected between the output of the positive peak reader and the negative peak reader will actually read the peak-to-peak value, as the difference between those two potentials. The voltmeter may not be grounded, however, and should be a true differential device.

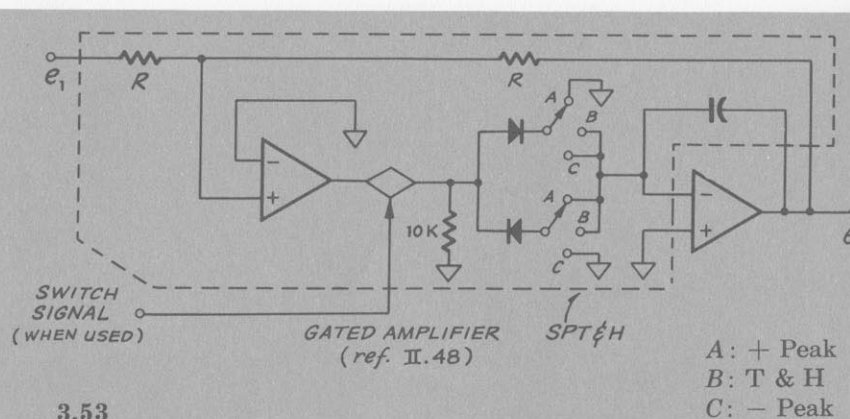
3.52



III.52  
I.32  
I.33  
I.34  
II.1  
II.2  
II.3  
II.36  
to  
II.40  
II.46  
to  
III.53  
III.74

**III.53 TRACK—HOLD—PEAK READER.** When the selector switch is in the B position, the circuit functions in exactly the same manner as the gated track-hold circuit of II.48. When the selector switch is in the A position, the integrator is not permitted to track positive-going input signals, because they are automatically shunted to ground through one of the diodes. Only negative-going signals are tracked, and then only the most negative signal is held, for the gated amplifier will receive a negative signal at its input (the resistive summing point) only when the input is more negative than the output is positive. Similarly, when the switch is in the C position, positive-going peak input signals are tracked, and negative-going input signals are ignored. Note that there is a net inversion; the circuit really tracks and holds the *negative* of its input.

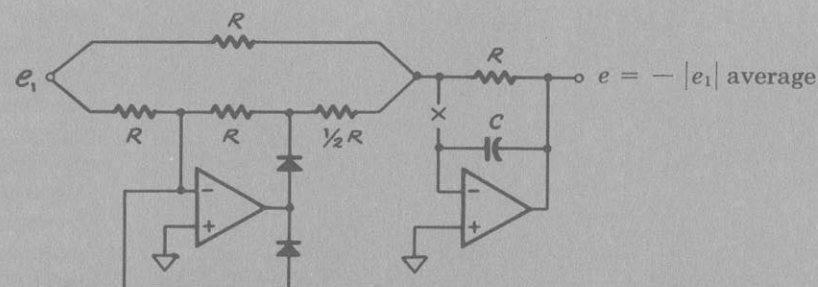
3.53



III.53  
I.32  
I.33  
I.34  
II.1  
II.2  
II.3  
II.36  
to  
II.40  
II.46  
III.52  
III.74

**III.54 PRECISE AC AVERAGE READER.** Refer back to II.42, Circuit (b)—the Precise Absolute Value Circuit. This circuit is identical to it, except that the capacitor C "averages," or smooths, the output voltage into a DC value almost exactly equal to the rectified average value of  $e_1$ . There are no appreciable diode errors of any kind in this "perfect" rectification. Furthermore, if the circuit is opened at point "x," the output will remain at whatever value it had at the instant of opening . . . at least, until the capacitor has discharged appreciably. A word of caution—unless the averager has a sufficiently long time-constant, the value that it "remembers" will depend upon the particular instant in the cycle of  $e_1$  at which the circuit is opened. On the other hand, if the circuit has a long enough time-constant to eliminate ripple, its response to a change in the "envelope" magnitude of  $e_1$  will be sluggish, and will require many cycles of  $e_1$  to settle to a new value. This means that the "true average" exists only when the waveform of  $e_1$  has been at equilibrium for a very long time . . . which may never happen.

3.54



Averaging Time Constant =  $T = RC$

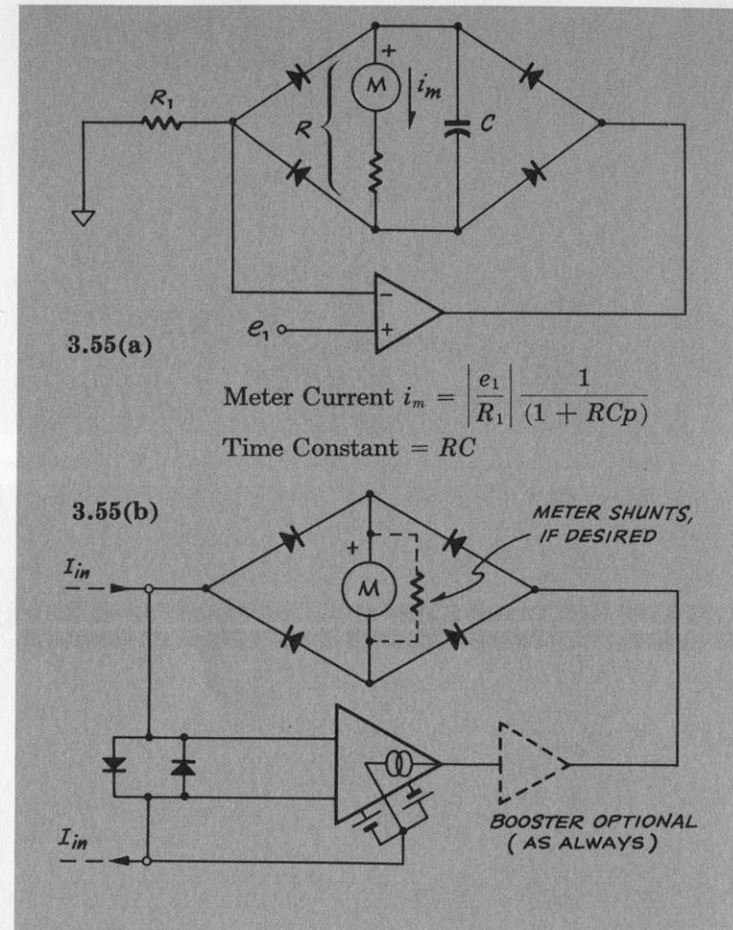
III.54  
II.10  
II.11  
II.12  
II.41  
III.55  
III.63  
III.65  
III.81

### III.55 PRECISE AC MILLIVOLTMETER AND "ZERO-DROP" MILLIAMMETER.

In circuit (a), a follower-with-gain is provided with a rectifier bridge as its feedback element. The amplifier forces the voltage across  $R_1$  to track  $e_1$  perfectly . . . ignoring the usual Departures From The Ideal. In order to do this, it must drive a current equal to  $e_1/R_1$  through the bridge. By the courtesy of the rectifier diodes, this alternating current is rectified into DC, averaged by the capacitor  $C$  in accordance with the time-constant given on the drawing and displayed on the DC meter  $M$ . The rectification is precise (perfect) because the output voltage of the amplifier accommodates any and all of the rectifier diode idiosyncrasies in its determination to track  $e_1$ . This circuit, when equipped with a reasonably sensitive meter, may have a remarkably high sensitivity, and yet present nearly infinite impedance to the signal, compared to a conventional millivoltmeter.

Circuit (b) approaches the ideal of a zero-energy AC milliammeter, because the drop across its terminals is virtually zero . . . except

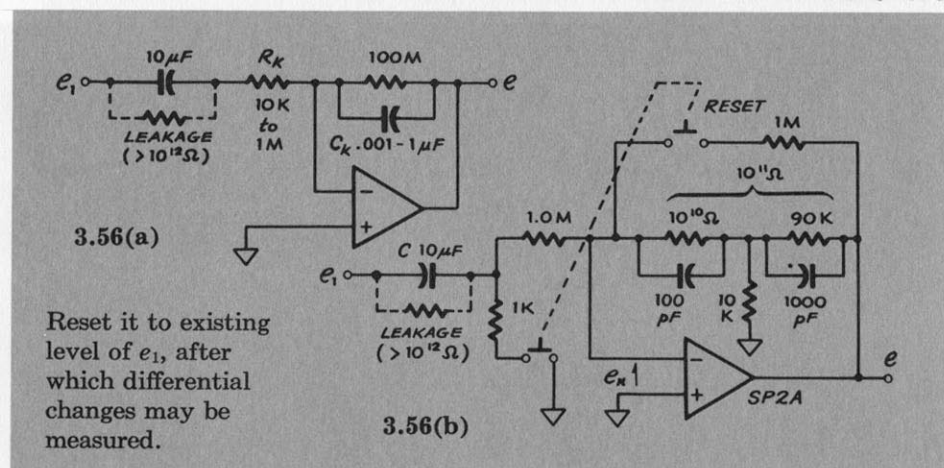
for the usual Departures. The input current must flow directly into the summing junction, and, provided that neither the amplifier nor the diode clamps draw any significant current, the current through the bridge that forms the feedback network must have the same value. The return path for this current is through the amplifier output terminal, and back to the source, through the amplifier "common." Provided that the amplifier output current rating is not exceeded, and that the output voltage swing required of the amplifier, as it forces the bridge current to track the input current, does not exceed its rating, the meter will read the true and precise rectified value of  $I_{in}$ , "averaged" by the inertia of the meter movement. Since this circuit has negligible drop, it is practical to convert it to a precise low-impedance millivoltmeter, by connecting in series with either input terminal, a resistor of appropriate size. Even at 10 mV full-scale, the null voltage error should be negligible compared to the error in the meter movement. For a high impedance millivoltmeter, however, circuit (a) is preferable.



**III.56 LONG-TERM DIFFERENTIATOR.** Circuit (a) is a practical differentiator with a characteristic time of 1000 seconds.  $R_k$  and  $C_k$  are stabilizing elements (see II.18, et al) and the  $10^{12}\Omega$  leakage is well tolerated (as are amplifier input current and stray leakage) by the 100 M feedback. To fix the order of magnitude, note that  $de_1/dt = 1 \text{ mV/sec.}$  produces  $e = 1 \text{ volt!}$

Circuit (b) adds to our study of this extreme circuitry the need for reset (shown in the simplest form) and the means for extending the time-constant far above 1000 seconds. If  $10^{12}\Omega$  is the best we can do in limiting the leakage, and if some "room" must be left for  $i_{in}$  and strays, then a feedback-network resistance of  $10^{10}\Omega$  is just about all we dare use; however, the Tee Network ( $90 \text{ K}/10 \text{ K}$ ) will buy us yet another order of magnitude, so that  $T = 10^6$  seconds—not quite two weeks! Think of it: 1 microvolt/second in, for one volt out!

There is no merit in increasing  $C$ —the leakage will rise just as rapidly. Reducing  $C$  will only partly help, because then  $e_n/R$  will begin to dominate. The optimum value lies between 1.0 and  $10 \mu\text{F}$ .



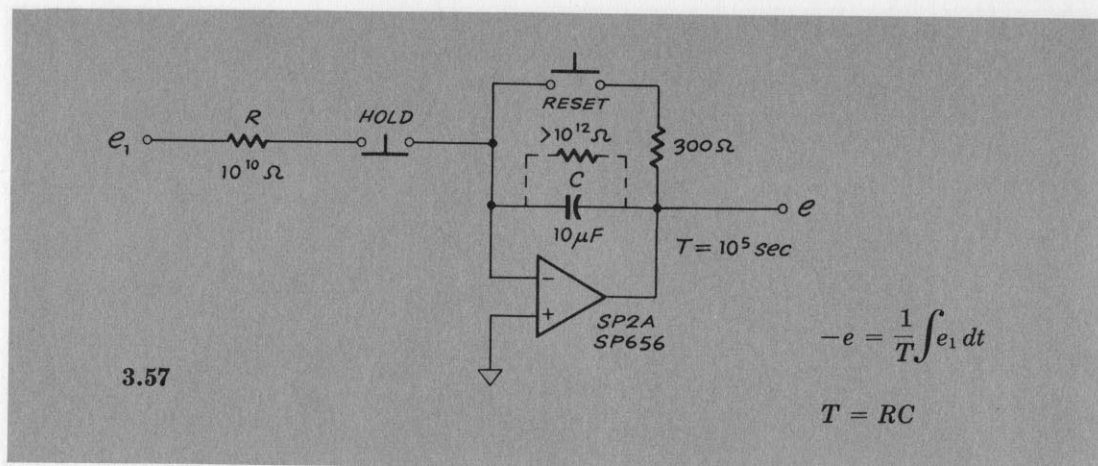
III.55  
II.1  
II.2  
II.3  
II.4  
III.54  
III.63  
III.65  
III.81

III.56  
I.7  
to  
I.18  
I.33  
I.34  
I.36  
II.18  
to  
II.21  
III.57



**III.57 LONG TERM INTEGRATOR—MEMORY.** This circuit takes full advantage of the very low offset current and voltage of a superior (Philbrick) modern (Philbrick) solid-state Operational Amplifier. Even at 10 volts full-scale, the input current is  $10^{-9}$  amperes . . . yet an accuracy of better than 1.0% may be anticipated—with a characteristic time of more than a day! (By the way, the limiting factor is capacitor leakage, *not* the amplifier offsets!)

Other *caveats*: Beware of stray leakage (select good insulation, and guard critical paths); noisy ground returns (see I.30); and stray coupling (see I.31).

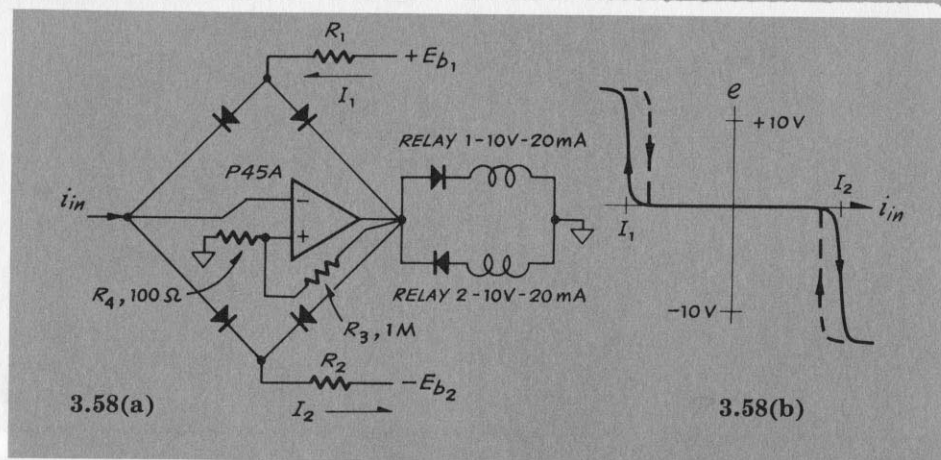


3.57

III.57  
I.7  
to  
I.18  
I.33  
I.34  
I.36  
II.10  
II.11  
II.12  
III.56  
III.73

**III.58 NULL DEVIATION WITH 3-GRADE SORTING.** This circuit has three possible states: (1) neither relay actuated; (2) relay 1 actuated; (3) relay 2 actuated. In state (1), normally-closed contacts on each relay, connected in series, “choose” the middle-grade-bin actuator—a condition corresponding to values of  $i_{in}$  that are smaller in magnitude than either  $I_1$  or  $I_2$ . The output/input relationship is like that of the Dead Zone circuit of II.44 until  $i_{in}$  exceeds  $I_1$  or  $I_2$  in magnitude; after which, the loop opens and a rapid transition occurs in the output voltage, actuating relay 1 or relay 2. This output/input relationship is shown in (b).

$R_3$  and  $R_4$  provide “latching” through hysteresis, as shown by the dashed lines in (b).



3.58(a)

3.58(b)

III.58  
I.25  
I.27  
II.1  
to  
II.4  
II.30  
II.41  
III.43  
III.44  
III.45  
III.47  
III.48  
III.78

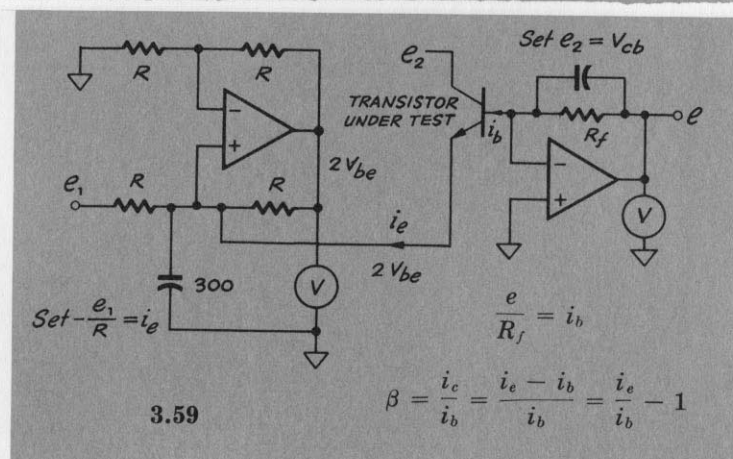
**III.59 PICOAMPERE TRANSISTOR PARAMETER TEST SET.** Here we see the practical application of two familiar circuits to the testing of transistor parameters at pico-ampere current levels. The circuit to the right of the transistor, which is nothing more than the current-to-voltage transducer described in III.30, permits us to measure very low base currents conveniently and accurately, with a voltmeter that reads its output,  $e$ . The base current is then known:

$$i_b = \frac{e}{R_f} \quad (3-23)$$

The emitter current is accurately established

and maintained by the use of the Howland Circuit (III.6), so proportioned that the voltage read on the voltmeter is exactly twice  $V_{be}$ . (Note that the amplifier in the base circuit operates to maintain the base essentially at ground potential.) The emitter current is programmed by the input voltage to the Howland Circuit, according to the relationship  $i_e = e_1/R$ .  $V_{cb}$  is set by adjusting  $e_2$ . Note that this configuration provides a convenient means of measuring the “DC Beta” of high-gain transistors, with negligible approximation error:

$$\beta = \left( \frac{e_1}{e} \right) \left( \frac{R_f}{R} \right) - 1 \quad (3-24)$$

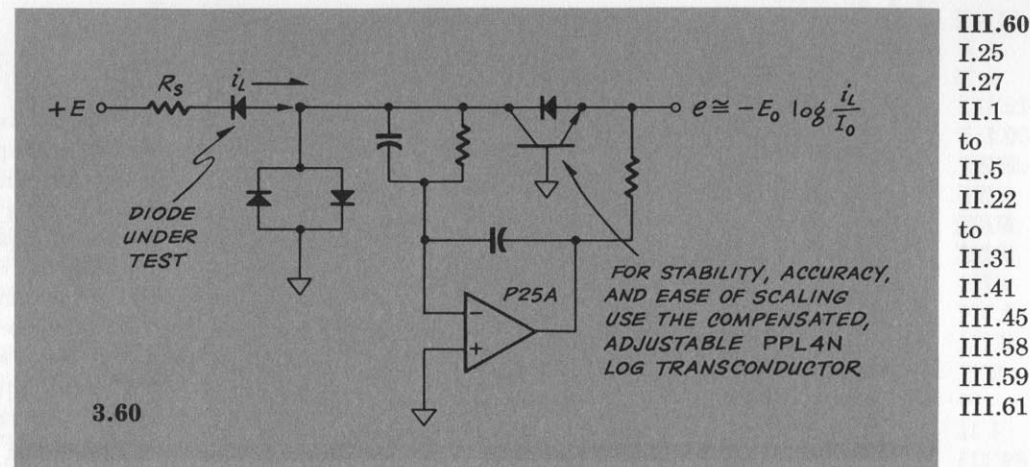


3.59

III.59  
II.1  
to  
II.5  
III.3  
III.4  
III.5  
III.6  
III.7  
III.8  
III.30  
III.60  
III.61

**III.60 DIODE-TRANSISTOR LEAKAGE MEASUREMENT.** The logarithmic-response null amplifier circuit of III.45 may be used to advantage in the measurement of very small diode or transistor leakage values. (A logarithmic characteristic is desirable since leakage values frequently vary, from diode to diode, over many decades. To protect against the occasional shorted or leaky diode, back-to-back diode clamps are shunted across the input to the circuit, and  $R_s$  is used to limit the current fed to them. A compensated, adjustable, logarithmic transconductor may be used here for accuracy, temperature independence, and gain adjustability.\* The amplifier input terminal is deliberately decoupled from the diode clamps, to insure that they, and not the amplifier itself, limit first in the event of a shorted or very leaky diode. This circuit may be used to drive a recorder, a digital voltmeter, a conventional panel meter, or a limit comparator circuit (II.41 and III.58). It is well suited to automatic sorting of diodes or transistors.

\*Philbrick SPL4-N/P are recommended.

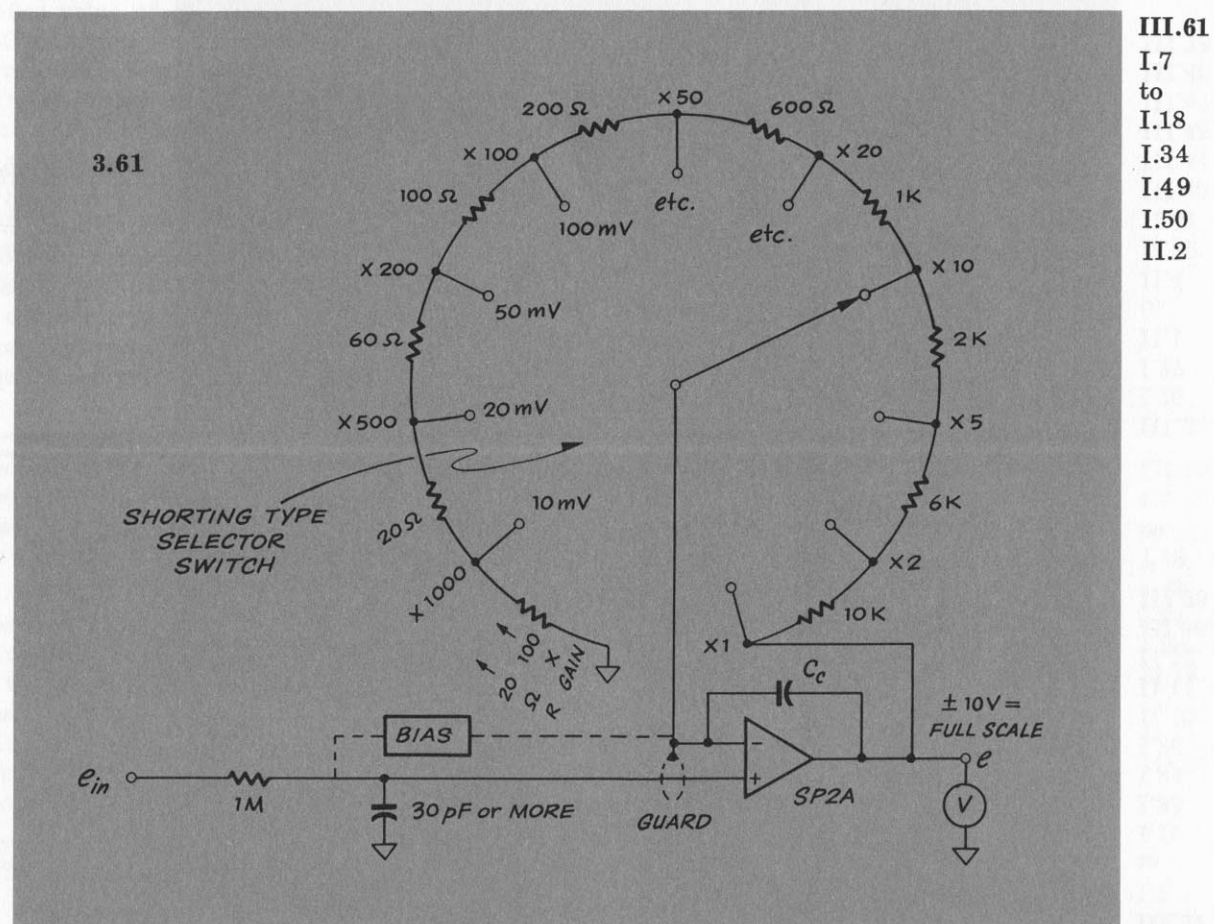


**III.61 ELECTROMETER—MILLIVOLTMETER—AMPLIFIER.** In this version of the Follower-With-Gain circuit, a  $\pm 10$  volt output with nearly 2 mA of current capability is developed from full-scale input voltages as small as  $\pm 10$  millivolts, while drawing less than 1 picoampere from the signal source. This exceptional sensitivity is made even more attractive by extremely high input impedance—ranging from at least 30,000 megohms (in the highest-sensitivity ranges) to millions of megohms (in the low-sensitivity ranges). The input impedance is actually the common-mode impedance of the positive input—in parallel with the differential impedance multiplied by the loop gain. With this order of input impedance (and appropriate care in construction), this circuit may certainly be assigned to the "electrometer" class, drawing currents of the order of  $10^{-11}$  to  $10^{-15}$  A. The input filter is provided to reduce noise and pickup, and both it and the compensating capacitor,  $C_c$ , are made as large as feasible to reduce the noise bandwidth without significantly slowing down the signal.

The "bias" current may be provided by a floating (cell) bias circuit (I.19, I.22) in series with a *very high* resistance, or by slightly offsetting the voltage bias, thus allowing it to develop an offset current through the amplifier's differential input resistance.

$$\left( \text{e.g., } \frac{10 \text{ mV}}{10^{10} \Omega} = 10^{-12} \text{ A} \right)$$

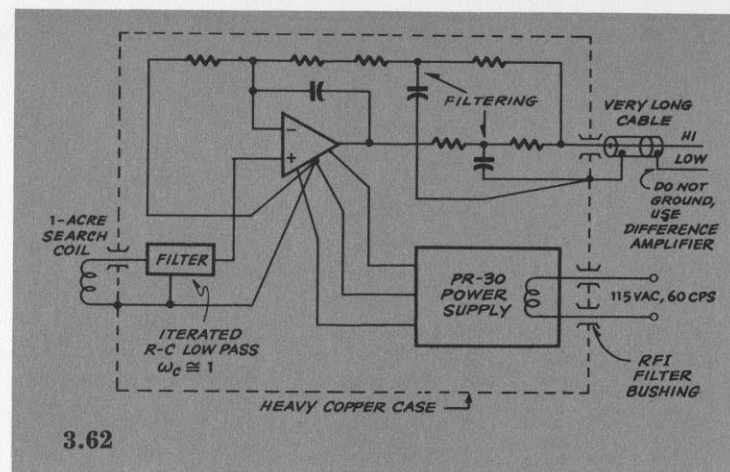
For less demanding applications, amplifiers of more modest performance at lower cost may be profitably employed.





**III.62 LOW-LEVEL MAGNETIC FIELD MEASUREMENT.** This unusual application illustrates the low-level capabilities of Operational Amplifiers and shows the precautions necessary when extremely small signals must be detected in the presence of large ground currents and stray coupling. The earth's magnetic field varies very slowly. Even a 10,000-turn search coil 6 feet in diameter will produce only 1.28 microvolts rms for a peak flux excursion of 10 microgauss (1 Gamma) at 0.01 kHz. The only saving grace is the fact that the bandwidth can be spoken of in terms of cycles per hour; which permits us to use filters to reduce the effective noise level, moving power line disturbances many octaves away.

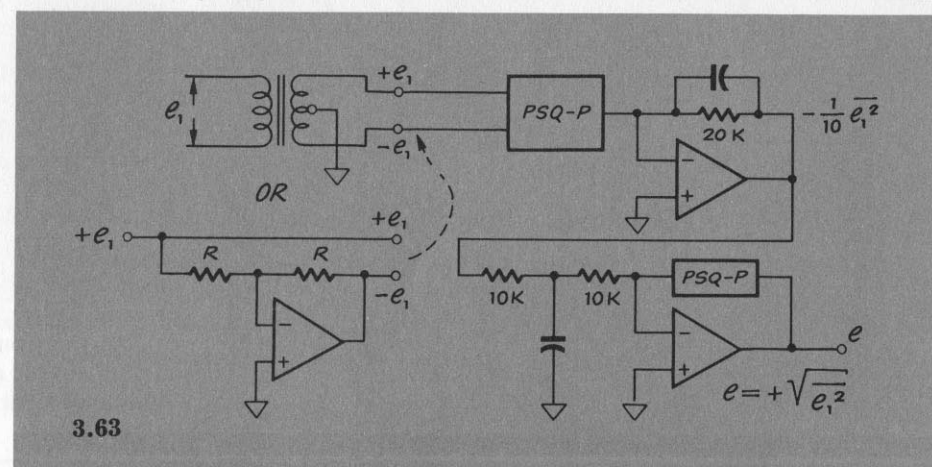
Note particularly: (1) the heavy copper case, for electrostatic shielding, and for some "shorted turn" effect on the incident power-frequency magnetic flux; (2) the "RFI filter bushings" used to lead signals in and out of the enclosure. Typical designs are the Sprague Type IJX 179 for the power lines and Type IJX 152 for the signal lines; (3) the use of an ungrounded coaxial cable for the output lead. If the cable is buried in the ground, it should serve as the signal return lead, and no other ground connections should be made. If the cable is not buried, the case should be grounded. Note that the input drives the positive terminal, and the amplifier is connected as a follower-with-gain.



III.62  
I.7  
to  
I.18  
I.28  
to  
I.31  
I.50  
II.1  
to  
II.4  
III.22  
III.23  
III.24

**III.63 TRUE RMS VALUE READER.** Here we feed the signal and its inverted value into a voltage-squaring circuit employing the PSQ-P Quadratic Transconductor (see II.24 et al), averaging the squared output to obtain the mean square of the input waveform. We show alternate forms of obtaining  $e_1$  and  $-e_1$  from  $e_1$  alone: a center-tapped transformer, and a unity-gain inverter.

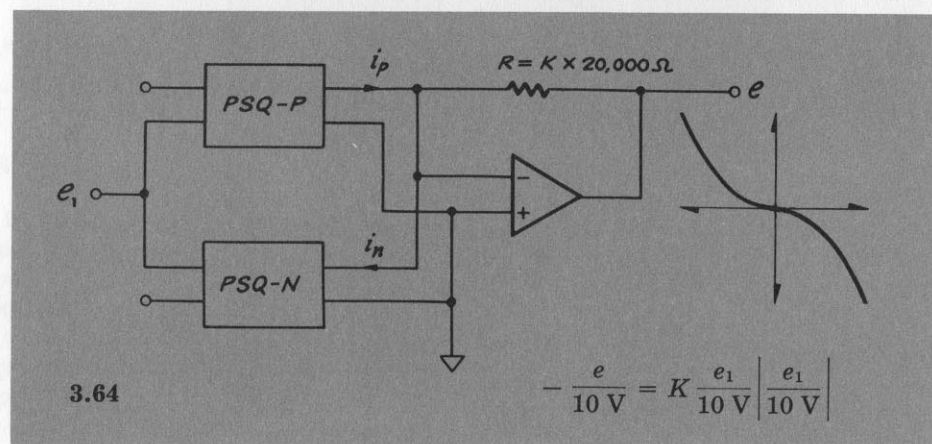
After filtering, the output of the averager is then fed to a square-root circuit, which employs the PSQ-N Transconductor (II.23, et al) so that the output  $e$ , of this last circuit is the square root of the mean square of  $e_1$ , otherwise known as the true RMS value of  $e_1 \dots$  over a frequency range extending from zero well up into the audio spectrum. The square root and elementary filter circuits shown may be replaced by an integrator (II.10) for true continuous-accumulation (total energy) measurement.



III.63  
II.22  
to  
II.32  
III.54  
III.55  
III.65  
III.81

**III.64 ODD-VALUE SQUARER.** The output of this circuit is proportional to the negative of the product of the input signal and the absolute value of the input signal—always in either the second or the fourth quadrant, as shown in the graph to the right. The constant  $K$  is proportional to the value of  $R$ . (For the standard Philbrick Quadratic Transconductors shown,  $K = 1.00$  when  $R = 20,000$  ohms.) As for the circuit, the so-called "ab-square," it consists of our old friend the current-to-voltage transducer, driven by the output current of one or the other of the Quadratic Transconductors. Positive values of  $e_1$  will produce negative output voltages, and negative values of  $e_1$  will produce positive output voltages. The current provided by the transconductor is proportional to the square of  $e_1$ , as is the resultant output voltage. The inverse of this function—the odd-value root, or "ab-root"—can be generated by interchanging the input and feedback elements.

Applications include: simulation of bidirectional hydraulic turbulent friction, synthesis of quadratic nonlinear conductance, creation of a graduated null or graduated dead-zone, or (when connected in the feedback path for odd-value rooting) synthesis of quadratic impedance.



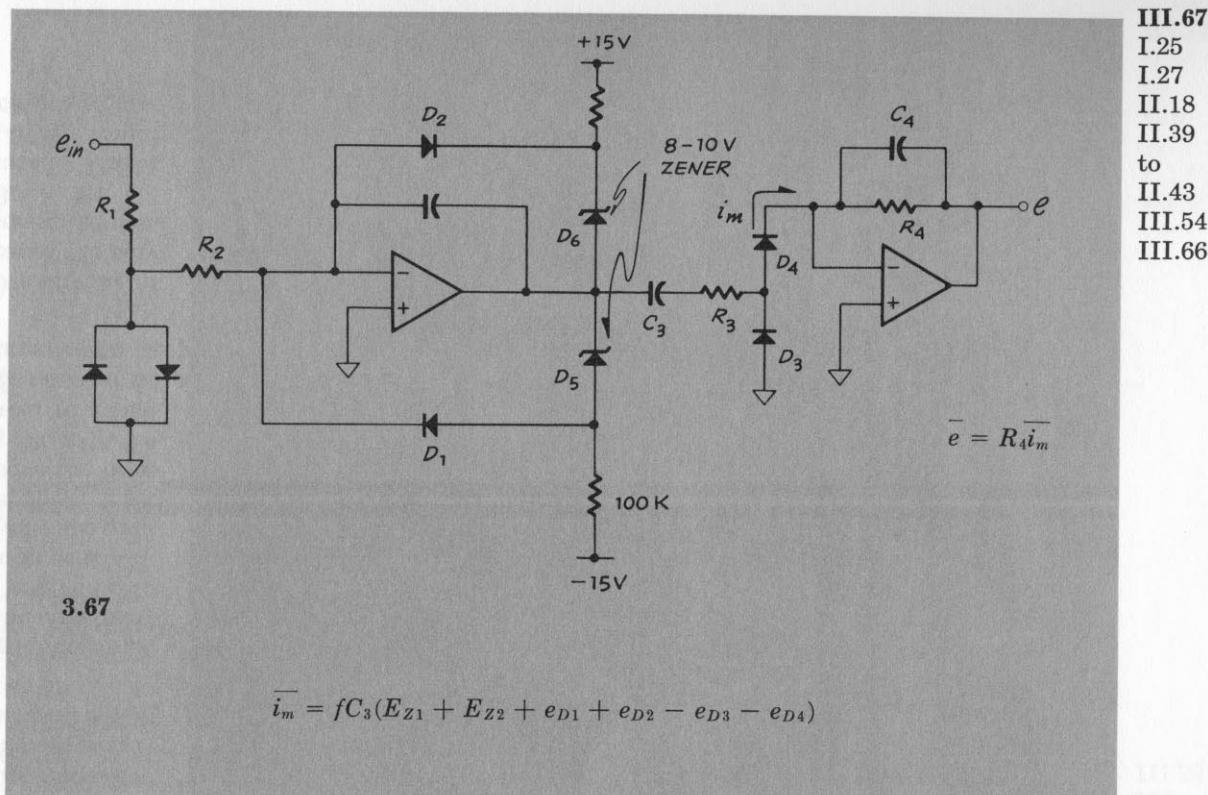
III.64  
II.22  
to  
II.32





**III.67 LOW FREQUENCY METER-CONVERTER.** This circuit is a low-frequency version of the preceding one (III.66). The bounded open-loop amplifier to the left produces a trapezoid of very steep sides (for low frequencies) and an amplitude of 16–20 volts. This waveform then produces “spikes” or pulses of current through  $C_3R_3$  (proportioned as in III.66) and these are “averaged” by  $C_4$  in the modified current-to-voltage transducer, which then drives a meter or other load.  $e$  is proportional to frequency *only*, for a given set of component values, as shown in the equations on the diagram.

The feedback capacitor shown connected around the main amplifier is of critical importance and must not be made too small, lest overshoot and effective distortion occur.



**III.68 DERIVATIVE  $dy/dx$  FROM TIME DERIVATIVES.** If  $e_x$  and  $e_y$  are *increasing* functions of time, so that their time-derivatives are positive,\* they will drive input currents into each of the logarithmic-response amplifiers to the left of the Subtractor. The output of each amplifier will, then, be proportional to the log of its input current—i.e., to the log of the time-derivative of the corresponding input voltage.

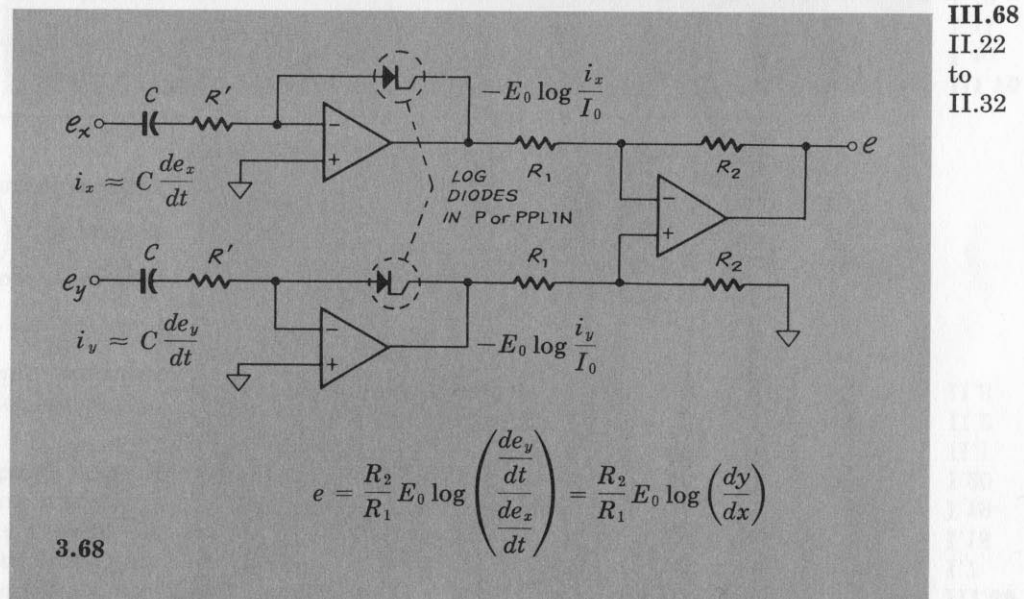
The Subtractor stage produces an output proportional to the *difference* of the logarithms, or proportional to the logarithm of their *ratio*, as indicated.

An anti-log circuit (see II.23) might be tacked on, at this point, to produce a signal of the form:

$$e' = K \left( \frac{dy}{dx} \right) \quad (3-26)$$

$R'$  is proportioned: (1) to achieve stability (see II.18, et al); (2) to prevent excessive capacitive loading of the input; and (3) to be as small as possible, yet still satisfy (1) and (2).

\*Both  $i_x$  and  $i_y$  must be positive (or both negative if the log diodes are reversed), since the logarithm of a negative quantity is not real.

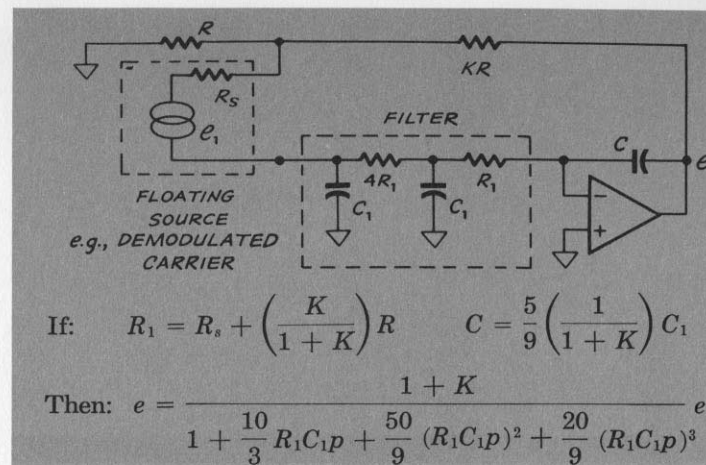


**III.69 DEMODULATOR-AMPLIFIER.** This circuit provides gain, impedance-buffering, and effective carrier filtering with reasonably fast envelope response for almost any kind of demodulator that can “float.” The demodulator impedance ( $R_s$ ) should be low enough to preserve the filter dynamics. This circuit permits one to insert a correcting bias (or an arbitrary “set point”) of appropriate polarity in series with the positive-input return to ground of the (differential) amplifier, without influencing the gain . . . a useful feature.

Note that the source impedance does not affect the low-frequency gain ( $1 + K$ ) but does make the amplifier current offset more significant.

The circuit has the further advantage of providing an independent gain control, in the form of an adjustment of the feedback resistor (or the feedback divider ratio) thus making it possible to adjust both the sensitivity and the initial zero independently.

The filter characteristic has been chosen to provide a minimally-overshooting transient step response, low phase shift ( $\phi \approx \frac{10}{3} R_1 C_1 \omega$ ) at low frequencies and high attenuation at high frequencies ( $\left| \frac{e}{e_1} \right| \approx \frac{9(1+K)}{20(R_1 C_1 \omega)^3}$ ). It is near optimum in these regards for an attenuation of 1000 at the carrier frequency.

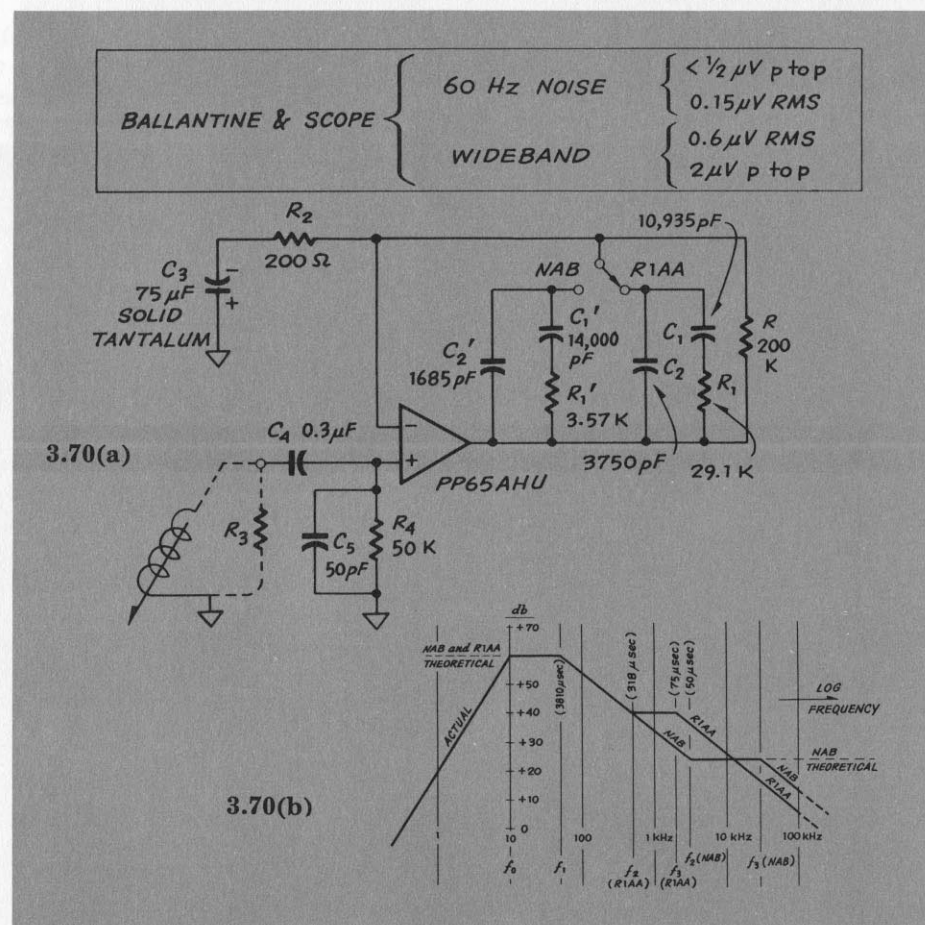


**III.69**  
I.7  
I.18  
I.19  
I.20  
II.1  
II.2  
II.3

**III.70 PHONO & TAPE PREAMPLIFIERS.** This circuit will be recognized as a form of follower with gain (see II.2), three features of which are important to this application. First, the amplifier's input resistance is well over 50 megohms, shunted by less than 20 pF. Second, the noise will be very low, especially important at low frequencies, where the input is smallest. Third, the frequency response is determined by the feedback network alone, and not by the amplifier; thus the calculated network values will be accurate to within a small fraction of a db.

Two standard equalization curves are shown—the RIAA for phonograph records, and the NAB for tape recordings. They require that the gain of the equalizing preamplifier begin “rolling off” at some frequency,  $f_1$ , at 6 db per octave up to another frequency,  $f_2$ . From  $f_2$  to a higher frequency,  $f_3$ , the gain is constant. Above  $f_3$ , the gain rolls off again, indefinitely, for RIAA. For NAB, the gain should be constant above  $f_2$ , indefinitely; however, to minimize noise, most audio equipment manufacturers arbitrarily roll off the response above the limit of hearing . . . beginning, say, at 30 kHz, as is shown here for  $f_3$  (NAB). To minimize low-frequency noise, especially transients, it is advisable to reject “DC” and low-frequency signals below some arbitrary cut-off frequency,  $f_0$ , here selected to be 10.6 Hz. Two time constants,  $R_2 C_3$  and  $R_4 C_4$ , combine to provide a 12 db per octave attenuation below  $f_0$ .

The tantalum capacitor  $C_3$  will always charge to about 10 to 100 millivolts of DC in the polarity shown (if the amplifier is properly zeroed) because the tiny amplifier input current (DC) flows through  $R_4$  from ground. Low noise requires relatively low input-circuit impedance—hence the choice of 0.3  $\mu$ F for  $C_4$ , which, with  $R_4 = 50$  k $\Omega$ , provides the desired low-frequency cutoff. Direct coupling can be employed by eliminating the  $R_4 C_4$  filter, and the circuit would then present essentially “infinite” impedance; however, most pick-ups require a resistive load of about 50 k $\Omega$  (some as low as 5 k $\Omega$ ), hence  $R_3$ .



**III.70**  
I.40  
I.41  
I.42  
II.2  
III.35



### III.71 NEGATIVE-IMPEDANCE/ADMITTANCE CIRCUITS.

The circuits shown here exhibit, between the input terminal and signal ground, a negative impedance (or admittance)\* in that a positive-going signal results in a negative current flow. Such a condition, produced as it is by positive feedback, will immediately suggest to the battle-scarred circuit designer the possibility of at least conditional instability, if not outright oscillation. Indeed, either of these circuits can run the gamut of instabilities from sinusoidal ringing to flipping and flopping from one bound to the other. Circuit (a), used to create negative impedance ( $Z_n$ ) tends to be stable for small values of source impedance  $|Z_s|$  and is, therefore, said to be "short-circuit stable." Circuit (b), used to create negative admittance ( $Y_n$ ) tends to be stable for *large* values of  $|Z_s|$ , and is, therefore, said to be "open-circuit stable."

\*The reason for making this distinction in nomenclature will be apparent in a very few lines.

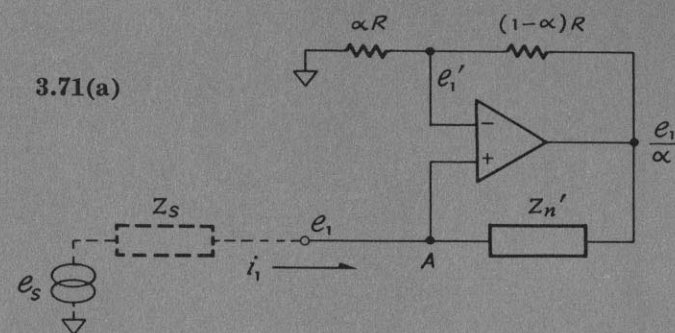
A necessary condition for stability for each circuit may be stated more rigorously as:

- Circuit (a),  $\left| 1 + \frac{Z_n}{Z_s} \right| > \frac{1}{\alpha} = 1 - \frac{Z_n'}{Z_n}$
  - Circuit (b),  $\left| 1 + \frac{Z_n}{Z_s} \right| < \frac{1}{\alpha} = 1 - Y_n Z_n'$
- (3-27)

for all values of frequency. However, even when (3-27) is satisfied, one cannot be certain of stability—in other words, the condition stated is not sufficient.

We have already seen one very useful application of these circuits, in III.37, which discussed the creation of a negative capacitance across the input-to-ground terminals, to neutralize input capacitance. It is apparent from the equations developed on the drawings that these circuits can develop negative resistance, capacitance, inductance, or combinations thereof, provided only that the stability requirements be respected.

3.71(a)



$$e_1 = e_1' \text{ (assuming infinite amplifier gain)}$$

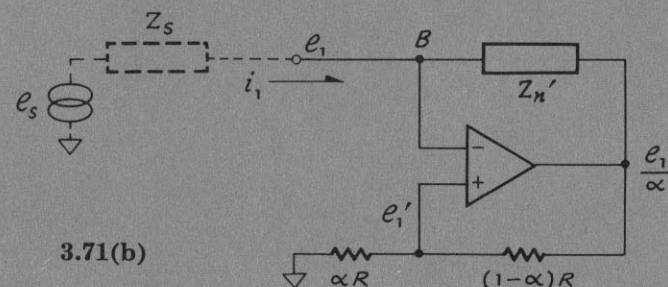
$$i_i = \left( e_1 - \frac{e_1'}{\alpha} \right) \frac{1}{Z_n'}$$

$$= -\frac{e_1}{Z_n'} \left( \frac{1}{\alpha} - 1 \right)$$

$$Z_n = \frac{e_1}{i_1} = -\left( \frac{Z_n'}{\frac{1}{\alpha} - 1} \right)$$

Negative Impedance,  $Z_n < 0$ .

3.71(b)



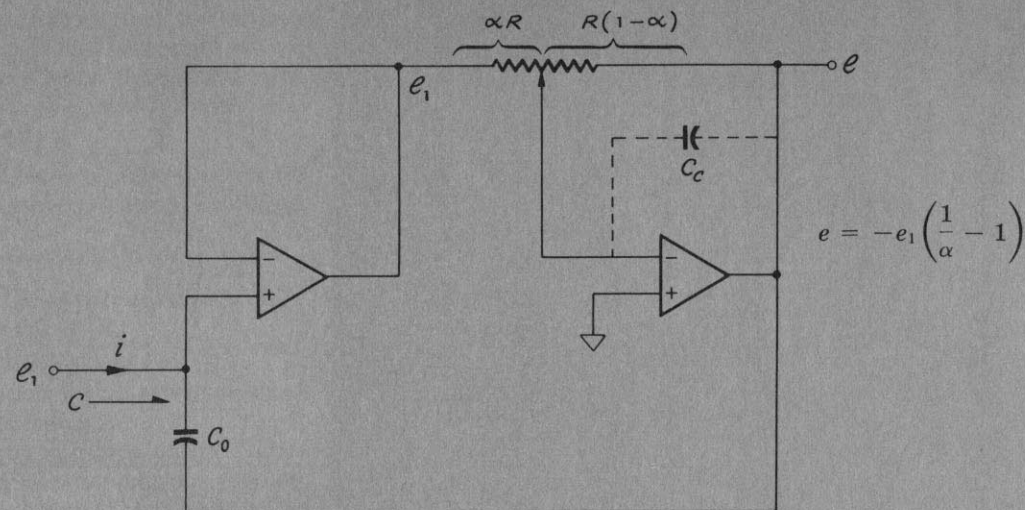
$$Y_n = \frac{i_1}{e_1} = -\left( \frac{\frac{1}{\alpha} - 1}{Z_n'} \right)$$

Negative Admittance,  $Y_n < 0$

III.71  
II.1  
to  
II.5  
III.6  
III.37  
III.72

**III.72 CAPACITANCE MULTIPLIER.** This circuit allows the synthesis of a capacitor or other impedance (between the input terminal and ground) that may be adjusted over a wide range by rotating the potentiometer shown, so as to adjust the gain of the inverter stage. The first stage is a simple follower, the only function of which is to isolate the capacitance created by this circuit from the loading represented by  $\alpha R$ . Indeed, if we have no objection to creating a "lossy" capacitor, and if  $\alpha R$  need never be adjusted near zero, the follower could well be omitted... but this circumstance is, unfortunately, rare. It will be noted that the capacitance created is inversely proportional to the rotation of the potentiometer, and it will further be noted that, since  $\alpha$  may be varied between 0 and 1, the input capacitance is always larger than, or at least equal to  $C_0$ . The principal limitation in applying this circuit to the construction of mammoth capacitors from tiny ones is that the ratio of  $e$  to  $e_1$  is almost exactly the same as the ratio of  $C$  to  $C_0$ , so that the larger the multiplication of capacitance achieved, the smaller is the maximum input signal that may be tolerated, for a given amplifier output-voltage rating.

Other limitations include: signal frequency, which must not exceed the value at which the finite-gain error factor intrudes upon the simple response relationship given here;  $Q$ , which is the function of the phase shift in the amplifiers, since such phase shift introduces a loss component, and noise components, which are magnified by the ratio of  $C$  to  $C_0$ .



$$\frac{d(e_1 - e)}{dt} = \frac{i}{C_0} = \frac{1}{\alpha} \left( \frac{de_1}{dt} \right)$$

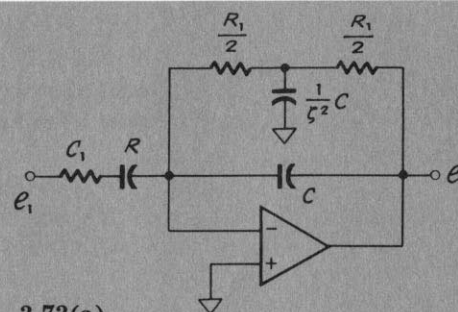
$$\text{Thus: } C = \frac{i}{\frac{de_1}{dt}} = \frac{1}{\alpha} C_0$$

3.72

**III.73 HIGH FIDELITY AC INTEGRATOR.** In this circuit, the conventional frequency response characteristic of an AC integrator (see II.11) is extended as shown providing accurate integration at lower frequencies, without loss of stability. This characteristic is accomplished by paralleling the integrating capacitor with a Tee network designed to roll off at approximately the same frequency as that at which the stabilizing Resistor and Capacitor, ( $R_c$  and  $C_0$  in II.11) would normally begin to limit the low-frequency response.

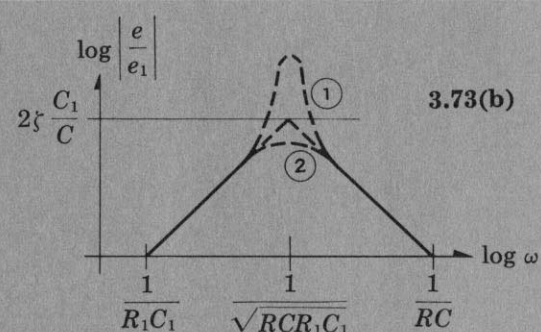
The same technique (with the  $R$ 's and  $C$ 's playing reverse roles) permits extended high frequency performance of a differentiator, while maintaining the noise-rejection capabilities at still higher frequencies. Both circuits are useful as second-order band pass filters, for  $\zeta$  (the damping ratio) not much smaller than 0.5.

This circuit has applications in instrumentation, e.g., the conversion of acceleration to velocity, velocity to position (or vice versa), etc.



3.73(a)

$$e = - \frac{e_1}{\frac{1}{R_1 C_1 p} + \frac{C}{C_1} + RCp} \quad \zeta = \frac{1}{2} \sqrt{\frac{R_1 C}{RC_1}}$$



Dashed lines ① and ② indicate typical underdamped and overdamped responses. Peak amplitude is  $\frac{C_1}{C}$

III.72  
II.1  
II.2  
II.3  
II.4  
II.5  
III.6  
III.37  
III.71

III.73  
I.26  
I.40  
to  
I.43  
II.10  
II.11  
II.12  
III.57



**III.74 PRECISION PEAK-READER/MEMORY.** This circuit will be recognized as a simpler variant of that of III.50, using only two amplifiers instead of three, at some (small) sacrifice of accuracy. The left-hand amplifier is used in a switching circuit of the type described in II.40. It responds only to negative input signals, being diode-bounded against positive inputs. Negative inputs are permitted to charge  $C$ , through  $R$ ,  $D_1$  and  $D_2$ . The voltage across  $C$  is the input signal for the second amplifier, which is connected as a unity-gain follower having two feedback paths:

(1) feedback through  $R_1$ , which creates, in effect, a unity-gain inverter, in combination with the input resistor,  $R_1$ . (The normal inverter summing-point equilibrium is achieved, however, *only* when and if  $C$  is charged fully to the instantaneous values of  $e_1$ ; otherwise, some current must flow through  $C_1$  and  $R_4$ .)

(2) feedback through  $R_2$ , which assists  $D_1$  and  $D_2$  in disconnecting  $C$  from any discharge path whenever the input voltage is the same as or less than the highest peak to which  $C$  has been charged since the last resetting. (Leakage in  $C$  itself, or through the reset push-button insulation, is not nullified by this expedient, however.)

The 10 M resistor provides a path for the leakage in  $D_1$ . The reset push-button restores  $C$  to the potential of the output of the switching amplifier, thus nullifying the error due to diode drop, particularly if  $R_3$  is made about equal to  $R$ . Initial conditions other than zero may be achieved by the method shown in III.49.

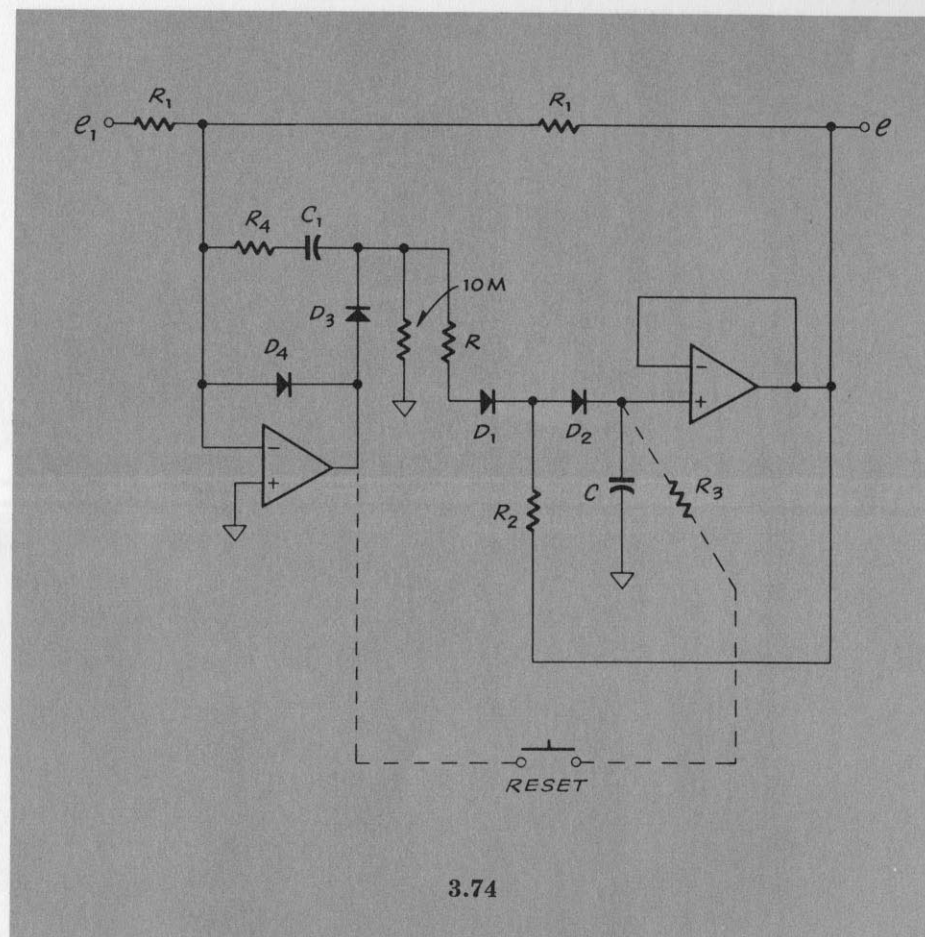
For good tracking  $RC$  should be *very* short compared to the fastest rate of change of  $e_1$ ; preferably an order of magnitude shorter. By reversing all of the diodes, the circuit can be made to track positive peaks, instead of negative. Note that the circuit inverts; that is,

$$e \text{ (a positive voltage)} = -E_p \text{ (highest negative peak of } e_1 \text{ since reset)} \quad (3-28)$$

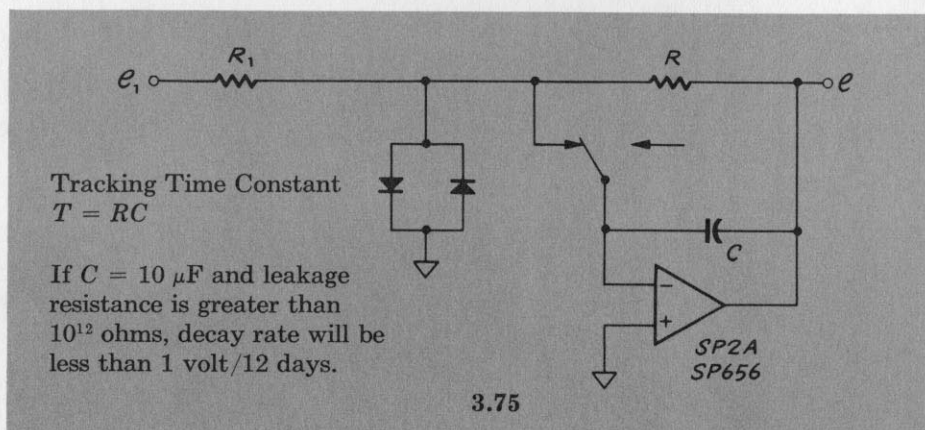
**III.75 TRACK-HOLD LONG-TERM MEMORY.** When the input to this circuit varies, the output "tracks" it, provided that the rate of change of output required does not exceed the limitations imposed by the tracking time constant,  $RC$ . (See II.46–48.)

When the relay contacts are open, the "Hold" Performance of the circuit depends almost entirely on the leakage in  $C$ , and only slightly upon the amplifier input current. The performance quoted in our exemplary diagram, while impressive, is not unusual for the best (Philbrick) amplifiers, polystyrene capacitors, and heads-up circuit construction.

There is the matter of resetting, which is automatically accomplished (back to "Track") by closing the relay contacts. The diodes are provided principally to keep the resistive summing point near ground potential during "Hold," whatever the range of input variation, thus tending to minimize voltage drop and hence leakage across the switch.



3.74



3.75

III.74  
II.39  
II.40  
II.49  
II.50  
II.51  
III.49  
to  
III.53  
III.75  
III.76

III.75  
II.39  
II.40  
II.49  
II.50  
II.51  
III.49  
to  
III.53  
III.74  
III.76

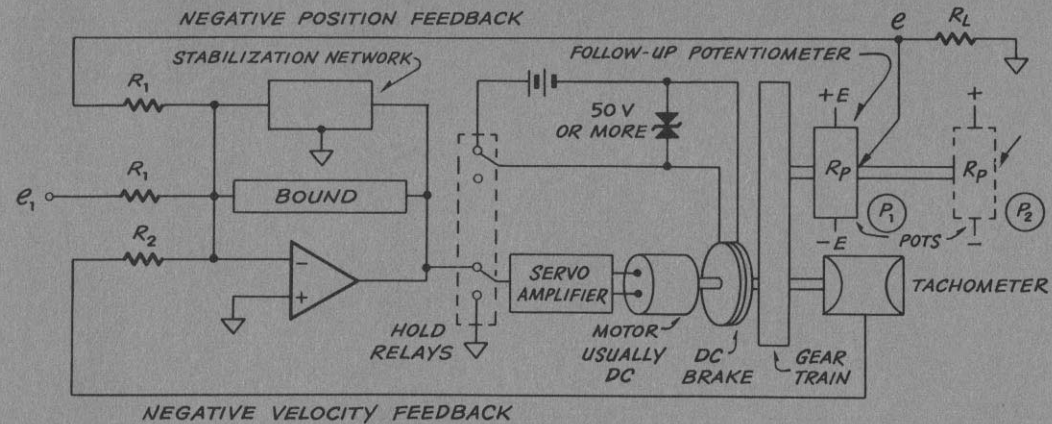
**III.76 PERMANENT TRACK-HOLD MEMORY.** This circuit, with the exception of the hold relays and brake, is representative of a servo-driven (computing) potentiometer of the kind used for multiplication, function generation, or trigonometric resolution. Tachometer (velocity or rate) feedback is incorporated to aid stabilization; although a tachometer may not be necessary if the output,  $e$ , is sufficiently noise-free to be differentiated to obtain a rate signal, as in (b).

The input must not change so rapidly that the output,  $e$ , is unable to follow it; therefore the time delay associated with relay operation and brake actuation should be small. The brake must be capable of rapidly dissipating the kinetic energy of the rotating parts. The zener clipping diodes in the brake solenoid circuit are used to reduce the magnetic field rapidly (by dissipating its energy) whenever the hold relay is opened. If the brake is spring loaded, it will always maintain the most-recently-servoed shaft position, even when the power is off. Note that the clamping accuracy of the brake is enhanced by the use of an anti-backlash gear train.

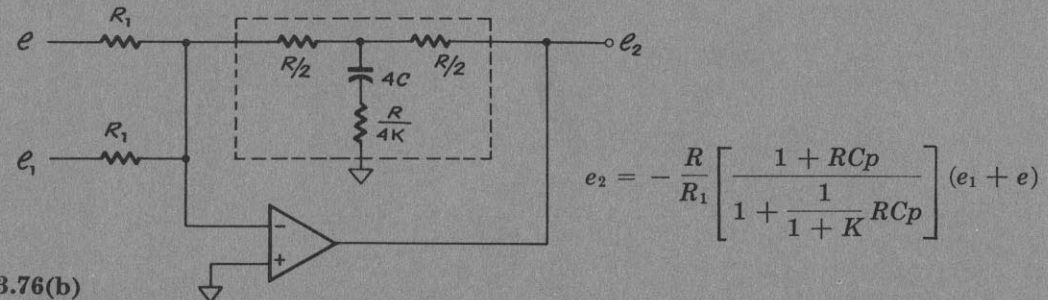
An additional follower-amplifier is needed if the output ( $e$ ) must drive a varying or heavy load ( $R_L$ ) since the potentiometer is loaded with the parallel resistance of  $R_1$  and  $R_L$ . If any other potentiometers are mounted on the same shaft as  $P_1$ , they should have the same resistance and electrical load as does the follow-up potentiometer, in order that their output voltages be proportional to  $e_1$ .

One may have to interchange the voltages ( $E$  and  $-E$ ), for net negative feed-back around the "position" loop.

3.76(a)

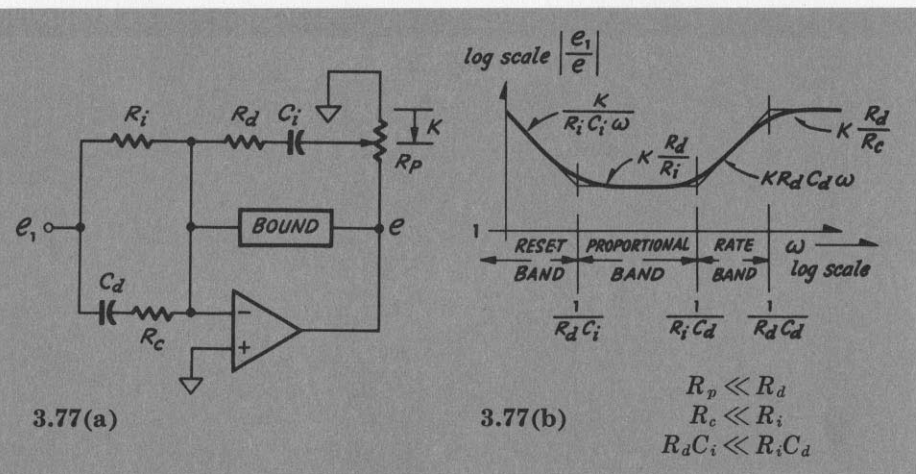


3.76(b)



**III.77 SIMPLE ONE-AMPLIFIER CONTROLLER WITH INDEPENDENT ADJUSTMENTS.** This controller circuit provides standard three-term proportional-derivative-integral control capability in a compact adjustable one-amplifier form convenient for many laboratory applications. Particularly useful is the ability of the bounding circuit (see I.25), to prevent "integrator wind-up" during periods of large error. As the sign of the error (input,  $e_1$ ) reverses, the output comes out of the bound immediately and begins to control the process.

In essence, this circuit is a combination of the augmenting differentiator of II.20, and the augmenting integrator of II.11.



III.76  
II.1  
to  
II.4  
II.41  
III.49  
to  
III.53  
III.74  
III.75

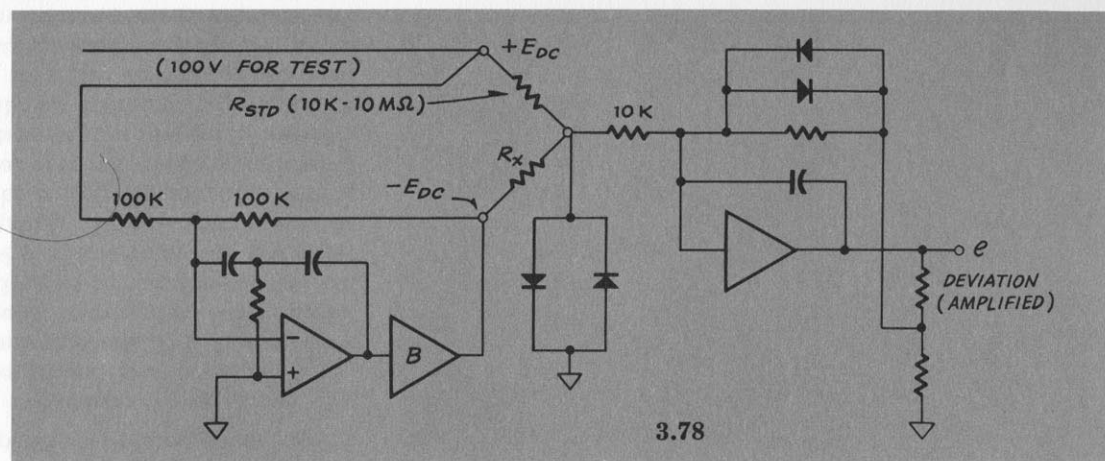
III.77  
I.40  
to  
I.43  
II.10  
to  
II.21  
II.44  
II.45



**III.78 PRECISION COMPARATOR.** The unity-gain-inverter circuit in the lower left of the drawing accepts the  $+E_{DC}$  test voltage, and creates its exact mirror image ( $-E_{DC}$ ) to drive the lower end of  $R_x$ , the unknown. If  $R_x = R_{STD}$ , and if the inverter feedback divider is perfect, then the input to the null-deviation detector circuit will be at zero, exactly. The output,  $e$ , of the detector will also be zero.

The detector output is bounded (to protect its meter load and avoid saturation) and its input is diode-clamped against such unnatural conditions as removal of  $R_x$ . For small deviations, this detector circuit is fairly linear, and may be calibrated for percent of deviation, or ohms of deviation.

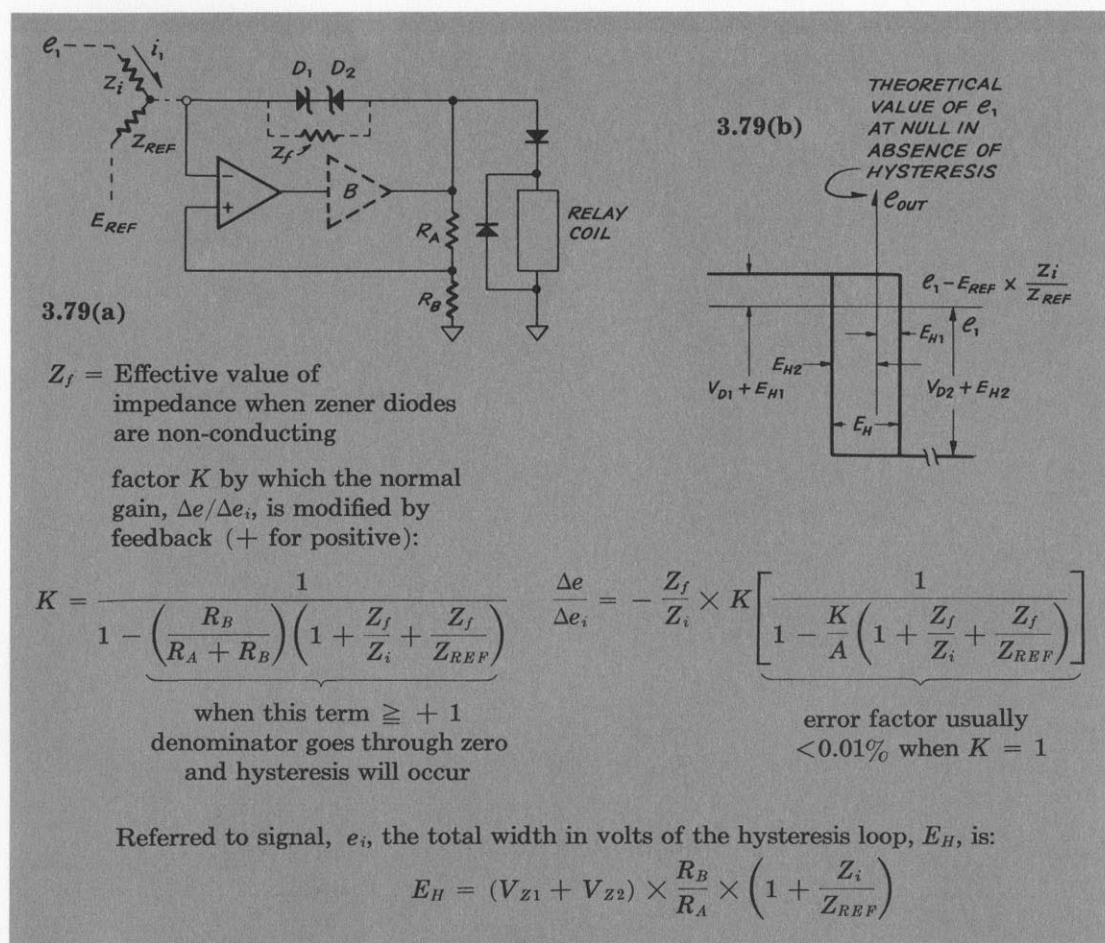
The null (match) point is unaffected by variations in  $E_{DC}$ , because of the "mirror-image" behavior of the inverter, but the calibration sensitivity is still directly proportional to  $E_{DC}$ .



III.78  
I.25  
II.1  
to  
II.4  
II.30  
II.41  
III.43  
to  
III.48  
III.58

**III.79 METERLESS "METER RELAY."** This circuit simulates a meter relay—that is, a moving coil relay in which the pointer of the meter in some way carries a contact, or has the ability to cause contact closure when its deflection reaches a specified value, in either direction around a center-zero position. Let us begin our analysis by mentally grounding the positive input terminal of the amplifier, instead of connecting it to the output divider  $R_A, R_B$ . Now the circuit will compare the potential at the junction of  $Z_1$  and  $Z_{REF}$  with ground, and any appreciable deviation, however small, will cause the output to bound at the voltage of the back-to-back zeners used as the feedback elements in order to maintain the summing point at zero. This swing to the bound condition will certainly cause the relay to operate. If the input signal range is small compared to noise (in  $e_1$ ,  $e_n$ , or  $i_i$ ) the output of the amplifier will swing wildly, which will in turn cause the relay to "chatter."

If, however, we now restore the positive input terminal to its proper tap on  $R_A, R_B$ , the positive feedback that results produces a "hysteresis" action quite similar to that produced by magnetically aided meter relay contacts—that is, once the circuit crosses the threshold, the positive feedback forces it the rest of the way, and holds it in the bound state until such time as the input signal comes back well beyond the forward threshold. By adjusting the positive feedback divider, the width of this hysteresis region may be varied. Note that the diodes in series with the relay are often not necessary, and should be omitted if bi-directional action is desired. Note also that the input signal need not be a voltage source, but may be a pure current source. The booster may not be required if the amplifier has sufficient current capacity to drive the relay. Figure (b) shows a typical hysteresis of the kind we have described. Useful design equations are given under the schematic.

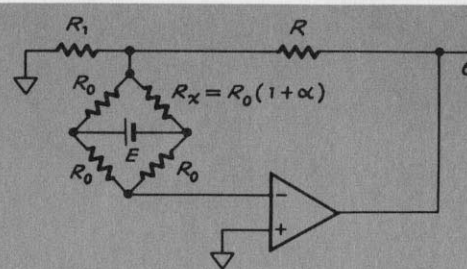


III.79  
I.25  
I.27  
I.44  
I.45  
II.1  
to  
II.4

**III.80 BRIDGE AMPLIFIERS.** Because of their inherent symmetry and self-duality, bridges are fascinating subjects for study. Here are four (out of many) popular approaches to the use of Operational Amplifiers with resistance bridges.

All but (d) are primarily used as small-signal (nulling) bridges, because of their nonlinearity in response to large deviations. Circuit (a) is the most convenient, because it may be used with a single-ended (possibly chopper-stabilized) amplifier, the sensitivity is independent of bridge impedance level (permitting indifference to common-mode bridge temperature variations), and the readout is proportional to the true voltage difference developed across the bridge—but the bridge-excitation supply must float . . . often a significant limitation. Circuits (b) and (c) are “galvanometric” bridges, in which the opposing corners are maintained at equal potential by the amplifier, which reads out the voltage required to establish the balancing differential current. If an accurately-tapped, stable power supply is available, (c) is better; otherwise (b) serves well, but one must choose an amplifier type insensitive to the potentially-large common-mode level. Bridge (b) could be read out potentiometrically by the use of circuit III.39, with consequent first-order independence of impedance level, for both scaling and common-mode rejection.

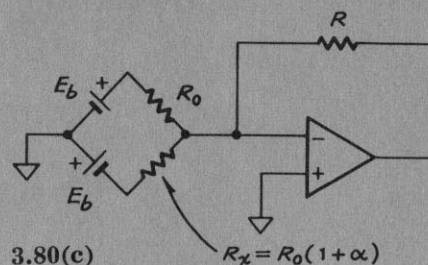
Bridge (d) is inherently linear, even for very large deviations; and it is used with a grounded supply—two major virtues. A further advantage of (d) is that its output is independent of bridge impedance level, as is that of (a). However, because (d) does not provide amplification, the measurement of small resistance changes may be difficult, unless another amplifier is added to increase sensitivity. Also, it is a 5-terminal “interrupted” bridge—one corner has been opened. This circuit configuration may not be realizable using a conventional bridge as the base for constructing circuit (d).



3.80(a) FLOATING SUPPLY

$$e = \left(1 + \frac{R}{R_1}\right) \frac{\alpha}{4 \left(1 + \frac{\alpha}{2}\right)} E$$

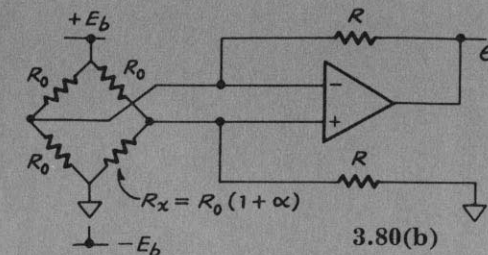
(Linear for  $\frac{\alpha}{2} \ll 1$ )



3.80(c)

GROUNDING BALANCED SUPPLY

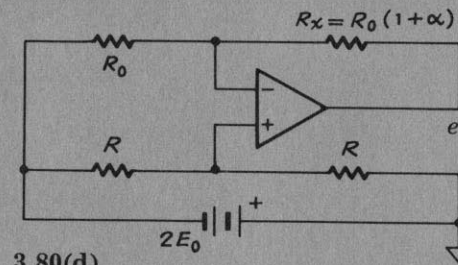
$$e = \frac{R}{R_0} \frac{\alpha}{1 + \alpha} E \quad (\text{Linear for } \alpha \ll 1)$$



3.80(b)

GROUNDING OR FLOATING SUPPLY, NOT NECESSARILY BALANCED

$$e = \frac{R}{R_0} \frac{\alpha}{1 + \alpha} \frac{E}{1 + \frac{R_0}{2R}} \quad (\text{Linear for } \alpha \ll 1)$$



3.80(d)

5-TERMINAL BRIDGE, GROUNDING SUPPLY LINEAR DEVIATION

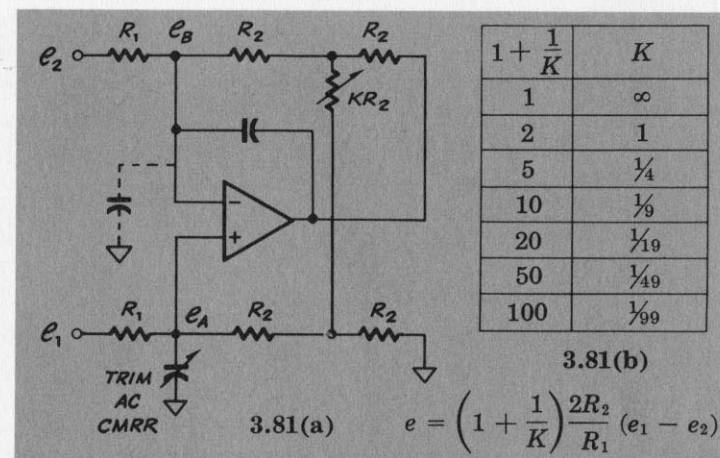
$$e = \alpha E_0 \quad (\text{No linear approximation})$$

**III.81 ADJUSTABLE-GAIN DIFFERENCE AMPLIFIER.** By using differential form of the Tee network (I.26), the gain of the difference amplifier (II.5) may be widely ranged by adjusting only a single resistor— $KR_2$  in (a). The common-mode rejection of the circuit is independent of this resistor; indeed, if the same (common-mode) voltage is applied to each input, and if all the resistors are symmetrically matched, the output will be zero.

Since the effect of  $K$  on gain is far from linear, gain variation with the rotation of a (linear) rheostat is also nonlinear (b). Linearity can be improved by putting a fixed resistor in series with the rheostat. This expedient will increase the gain at the minimum setting, for a given resistor ratio. An alternative is to use a multi-

position switch to select discrete values of  $KR_2$ , and thus specific calibrated gains (b).

The trimming capacitor shown from the positive input to ground may be necessary to ensure good common-mode rejection over a substantial range of frequencies. This capacitor should be adjusted to compensate for the net effect of all of the capacitances at the negative summing point. If the common-mode voltage varies substantially, an amplifier having a small and linear common-mode error should be used, so that trimming one of the  $R_1$  resistors will provide almost perfect rejection. A CMRR greater than  $10^6$  can be achieved at low and moderate frequencies with (a), if the inputs are driven from low impedance sources.



3.81(a)

$1 + \frac{1}{K}$	$K$
1	$\infty$
2	1
5	$\frac{1}{4}$
10	$\frac{1}{9}$
20	$\frac{1}{19}$
50	$\frac{1}{49}$
100	$\frac{1}{99}$

3.81(b)

$$e = \left(1 + \frac{1}{K}\right) \frac{2R_2}{R_1} (e_1 - e_2)$$









# APPENDIX

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Nomenclature.....	106-107
Symbology.....	108-109
Bibliography.....	110-111
Dimensional & Other Information.....	112
Philbrick Products and Services.....	113
Index.....	114-115
Solid State Amplifier Chart.....	116

# NOMENCLATURE

**Admittance:** For sinusoidal signals, the incremental ratio of a current to a voltage. A *self-admittance* describes the current-voltage relationship in a two-terminal element; a *driving-point* admittance relates the current into a terminal to the voltage between that terminal and common; a *trans-admittance*, in general, relates a current into any terminal of a circuit to a voltage between any pair of terminals.

**Arbitrary Function Fitter:** A circuit having an output voltage or current that is a presettable, adjustable, (usually non-linear) function of the input voltage(s) or current(s) fed to it.

**Bandwidth:** Generally, the frequency range over which a particular transfer characteristic (i.e., gain, attenuation, phase-shift, etc.) is maintained between two sets of terminals (i.e., input and output). In an Operational Amplifier, the frequency range over which the open-loop gain exceeds unity. In an Operational-Amplifier circuit, the frequency range over which the (small-signal) loop gain maintains the desired response, to the desired accuracy.

**Bias Circuit:** A (fixed or adjustable) circuit that is used to set amplifier (zero-signal) input-current or input-voltage level to an arbitrary value (normally zero). May be "temperature-compensating" . . . i.e., able to track the variation of amplifier input voltage or current with temperature, more or less perfectly.

**Booster Amplifier:** A circuit used to increase the output current or voltage capabilities of an Operational Amplifier circuit, without loss of accuracy (ideally) or inversion of polarity. Usually applied *inside* the loop, for accuracy.

**Bound Circuit:** A circuit designed to limit the excursion of a signal. The limit value it establishes may be nominal (when used for protection), or highly-precise (when used operationally).

**Chopper:** A circuit or device for interrupting (or at least modifying) a low-frequency signal path at a constant rate (i.e., carrier frequency), producing a wave, which is modulated by the DC signal magnitude, preserving the polarity of the DC signal. Generally associated with a *synchronous demodulator*, following amplification.

**Common-Mode Error (CME): (referred to the input)** A (generally) small offset voltage appearing between the input terminals of a differential operational amplifier, as a function of the *common-mode* voltage.

**Common-Mode Rejection Ratio (CMRR):** The ratio of common-mode voltage to common-mode error in a differential amplifier circuit.

**Common-Mode Voltage:** The voltage between the output signal return and (in this book) the positive input terminal of a differential operational amplifier.

**Comparator, Precision:** A high-gain amplifier circuit whose output changes decisively between two definite

levels whenever the sum of the input voltages changes sign.

**Controller:** A portion of a feedback system in which the unregulated unbalance (or "error") signal is operated on by adjustable dynamic elements (proportional, integral, derivative, lead-lag, etc.) to affect the manipulated variable in such a way that desirable response criteria for the loop (stability, speed, accuracy) may be met.

**Current Bias:** See Bias.

**Current Pump:** A circuit that drives, through an external (load) circuit, an adjustable variable or constant value of current, regardless of the reaction of that load to the current, within rated limits of current, voltage, and load impedance.

**Damping Circuit:** A circuit used to limit, control, or prevent dynamic instability (oscillation or "ringing") in a closed-loop active circuit, or in a complex passive network having appreciable second-order (or higher-order) response.

**Dead Zone:** A range in which no output change is produced by substantial input variations; a circuit element having such response (or lack of response).

**Differential-Input Amplifier:** One in which the output is (ideally) a function only of the *difference* between the signals applied to its two inputs, both signals being measured with respect to a common "low," or "ground" reference point.

**Differentiator:** Ideally, a circuit having a response (output) proportional to the time-derivative(s) of one or more input signals.

**Diode Bounding:** A form of *Bounding* in which the nonlinear conducting properties of a diode (or diodes) are used to accomplish the magnitude-limiting action.

**DC Beta:** The DC current gain of a transistor; the ratio of the collector current to the base current that caused it, measured at constant collector to emitter voltage.

**Drift:** A gradually-developing deviation in any voltage, current or impedance. For an Operational Amplifier, a gradually-developing change in the offset voltage or in either or both of the offset currents. Also, the bottom-most frequency range of the noise spectrum.

**Electrometer Amplifier:** An Amplifier circuit having sufficiently low-current drift and other noise components, sufficiently low amplifier input-current offsets, and adequate power and current sensitivities to be usable for measuring current variations considerably less than  $10^{-12}$  A.

**Emitter-Follower:** In principle, a single-transistor amplifier in which the load is connected between the emitter and signal ground, so that the base-to-emitter-to-ground path (for the input signal) contains 100% negative feedback of the output voltage. The collector is returned (in principle) directly to the power supply. The gain is very nearly unity and the output signal is *not* inverted (i.e., it "follows" the input).

**Error-Factor, Finite-Gain:** That factor by which the "ideal" closed-loop response expression must be multiplied to yield the response for an amplifier with *finite* gain, A, rather than infinite gain, as is assumed in computing the "ideal" response.

**Fault Current:** The current that may flow in any part of a circuit or amplifier under (specified) abnormal conditions.

**Follower-With-Gain:** A Follower (which see) in which only a *part* of the output voltage is fed back in series opposition to the input signal . . . hence, closed-loop gain greater than unity is obtained over the rated range of operation.

**Feedback Circuit:** A causal circuit configuration in which (for the simplest circuit) the input and the output variables are combined and together determine the output.

**Flicker:** Noise in an amplifier, of higher frequency than drift, but lower than power-line or chopper-drive frequency noise. Also called "jitter" or "wobble."

**Follower:** A circuit in which the output of a high-gain amplifier is fed directly back to its negative input. The input signal is reproduced without polarity reversal. See also Emitter Follower, and Follower with Gain.

**Flip-Flop:** See Multivibrator, Bistable.

**Frequency, Angular:** The rate of change of the angle of a sine wave, expressed in radians per second, where  $2\pi$  radians ( $360^\circ$ ) = 1 alternation (cycle).

**Frequency, Break:** In a plot of log gain (attenuation) vs. log frequency, the frequency at which the asymptotes of two adjacent linear slope segments meet.

**Gain-Bandwidth Product:** (1) The product of a specific frequency and the gain of a circuit, amplifier, or system *at* that frequency.

(2) For an Operational Amplifier, or any other circuit or device having the special property that its gain is inversely proportional to frequency, the G. B. P. is equal to the frequency at which the gain falls (by extrapolation) to unity.

**Gain, Closed-Loop:** The response of a feedback circuit to a voltage inserted in series with the *amplifier* input. Also the "noise gain."

**Gain, Loop:** In an Operational Amplifier circuit, the product of the transfer characteristics of all of the elements (active or passive) encountered in a complete trip around the loop, starting at any point and returning to that point.

**Gain, Open Loop:** The ratio of the (loaded) output of an Amplifier to its net input, at any frequency. Usually implies *voltage gain*.

**Gate, Precision:** A circuit that may be switched from closed- to open-circuit or vice versa without error (time, bias, impedance) in response to a command signal (voltage or current).



**Ground, Chassis:** The potential (assumed uniform) of the (metallic) structure on or in which the circuit is built.

**Ground, Power-Common:** The potential of the terminal or circuit point to which the output of a power supply (and often an amplifier output load) is returned (i.e., power-supply "zero").

**Ground, Signal (or High-Quality):** The potential of a terminal or circuit point to which all signal voltages are referenced, by convention or arbitrary assumption. Usually the signal-return of the lowest-level signal in a system.

**"Hold" Mode:** In integrators or other charge-storage circuits, a condition (or time-interval) in which input(s) are removed and the circuit is commanded (or expected) to maintain constant output.

**Hysteresis:** A form of non-linearity in which the response of a circuit to a particular set of input conditions depends, not only on the instantaneous values of those conditions, but also on the immediate past (recent history) of the input and output signals. Hysteretical behaviour is characterized by inability to "retrace" exactly on the reverse swing a particular locus of input/output conditions.

**Idling Current:** The zero-signal power supply current drawn by a circuit, or by a complete amplifier. Also called "Quiescent" current.

**Impedance, Input, Common-Mode:** The (internal) impedance between either one of the input terminals of a differential Operational Amplifier and signal ground.

**Impedance, Input, Differential:** The (internal) impedance observed between the input terminals of an Operational Amplifier.

**Impedance, Negative:** In general, the driving-point impedance of circuit in which a current increase produces a voltage decrease (and vice versa); for a *negative admittance*, a voltage increase produces a current decrease, and vice versa.

**Integrator:** A circuit having a response (output) proportional to the time-integral of one or more input signals.

**Inverter, Voltage:** A circuit having a response (output) proportional to a constant (the *gain*) times the input signal, but opposite in sign to it. In a unity-gain inverter, the output is  $(-1)$  times the input.

**Lag: (noun)** a delayed-response characteristic, or a circuit having such a delayed response. Usually 1st-order lag is implied unless otherwise specified.

**(verb)** to respond to a stimulus in delayed fashion.

**Lag-Lead (lead-lag):** A circuit whose response includes lag components and their derivatives.

**Leakage:** (Unwanted) current flow through a nominally-blocked (non-conducting) circuit or circuit element due to imperfections in its blocking behavior.

**Limits: (See Bounds)**

**Memory, Peak or Valley Readout:** A circuit in which the output remains at the condition corresponding to the

most positive (least negative) or vice versa input signal since the circuit was set to initial conditions, until reset to those conditions.

**Multiplier, Quarter-Square:** A circuit that achieves true four-quadrant multiplication by taking advantage of the mathematical relationship that the product of two variables is equal to one quarter of the difference of the squares of the sum and the difference of the variables.

**Multivibrator, Astable (free-running):** A circuit having two momentarily stable states, between which it continuously alternates, remaining in each for a period controlled by the circuit parameters, and switching rapidly from one to the other.

**Multivibrator, Bistable (Flip-Flop):** A circuit having two stable states, in either one of which it will stay indefinitely, until triggered appropriately, immediately after which it switches to the other state.

**Multivibrator, Monostable (one-shot):** A circuit having only one stable state, from which it can be triggered to change state, but only for a predetermined interval, after which it returns to the original state.

**Noise, amplifier:** All spurious or unwanted signals, random or otherwise, that can be observed in a completely isolated amplifier in the absence of a genuine input signal. (See also: Drift and Flicker.)

**Null Detector:** A comparator (which see) having zero reference voltage. A *graded-null* detector has decreasing sensitivity away from the null.

**Offset Current:** A DC error current appearing at either input terminal of a DC amplifier.

**Offset Voltage:** A DC error voltage appearing in series with either input terminal of a DC amplifier.

**Offset, End-Resistance:** In potentiometers, the residual resistance between a terminal and the moving contact, at a position corresponding to full rotation against that terminal.

**Passive Network:** A network whose net influx (or efflux) of available energy is stored or dissipated within the network. There may be no sources of energy other than those explicitly bookkept as influxes.

**Phase Characteristic:** A graph of phase shift vs. frequency, assuming sinusoidal input and output.

**Phase Shift:** Phase angle between two related variables in a circuit (usually input and output voltage) when excited by sinusoidal signal(s).

**Rate Limiting:** Non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)—restricting it to rates of change of voltage lower than might be predicted by observing the small-signal frequency response.

**Reset Mode (Set Mode):** In integrators, memories, or other charge-storage circuits, a state (or time-interval) in which the circuit is forced to return to a set of initial conditions, removing all record of its previous condition.

**RMS Value:** The square root of the time average of the square of a variable signal.

**Roll-Off:** The decrease in magnitude of gain with frequency. Typical roll-off (low-pass) of a circuit for which the dominant lag is first-order is 6 db per octave (inversely proportional to frequency). "Steep" roll-off might be at 12 or 18 db per octave (proportional to the inverse square or cube of frequency) or more.

**Saturation Voltage:** Generally, the voltage excursion at which a circuit self-limits . . . i.e., is unable to respond to excitation in a proportional manner. In Operational Amplifiers, the output-voltage saturation limits may be imposed by any stage, from the input to the output, depending in part on the external loading and feedback parameters.

**Scaling:** Adjusting the coefficient of a circuit to each of its one or more input signal terminals. The *relative* scaling (of one input to another) is called "weighting." In computing, relating problem variables to machine variables.

**Slewing Rate:** See Rate Limiting.

**Soakage:** The disability of a capacitor to come up to voltage instantaneously, without voltage lag or creep, during or after charging. The lower the soakage, the lower the lag and creep.

**Stabilizer: (DC)** A circuit that uses a chopper and preamplifier to maintain the net offset near zero at the input terminals of an Operational Amplifier. (See Chopper-Stabilized.)

**(Dynamic)** An element or circuit employed to promote dynamic stability, also *dampener*.

**Subtractor:** An Operational Amplifier circuit in which the output is proportional to the difference between its two input voltages (or between the net sums of its positive and negative inputs).

**Time Integral:** The definite integral of a variable over an interval of time. Also the area under a curve of a function of time during that period. Divide it by the time interval to obtain the average value of the argument over that period.

**Track-Hold Memory:** A circuit that, in its "track" mode, develops an output that follows (ideally) the input exactly, or is proportional to it; and then, in its "hold" mode, maintains the output constant (ideally) at the value it had at the instant the circuit was commanded to change from "track" to "hold."

**Transconductor:** A device that produces a current at a given point in the circuit (usually an amplifier's summing point) as a function of a voltage or voltages, usually at its input or output.

**Transdiode:** A transistor so connected that base and collector are actively maintained at equal potentials, though not connected together. The logarithmic transfer relationship between collector current and base-emitter voltage very closely approximates that of an *ideal* diode.

**Uncertainty, Input:** In an Operational Amplifier, the algebraic sum of all the factors, including environmental and time effects, that contribute to the non-ideal behavior of the input circuit. See Sections I.7-14.

**Weighting:** See Scaling.

# SYMBOLOLOGY

NOTE: This list includes terms used more or less frequently throughout the preceding pages, some of them in special senses. It omits familiar conventional symbols such as A (amperes), Hz (cycles/sec),  $\pi$  (3.1416), and  $\Omega$  (ohms). Specific references, where given, are to modules where the symbol is first, or characteristically, used. Such physical quantities as voltage, current, etc., are described by lower-case symbols when circuit variables, upper case when constants or magnitudes.

SYMBOL	TERM	UNITS	EXPLANATION
$A$	Gain		Operational Amplifier open-loop voltage gain
$A_0$	Gain		Same, at DC
$B$	Booster Amplifier Normalized Bandwidth  Bias Supply	Hz (cps) Radians/sec	See I.8
$C$	Capacitance, capacitor	Farads	Often with identifying subscripts e.g. $C_1, C_2$
$C_c$			Compensating capacitor
$C_L$			Capacitance of load, or capacitor that is part of load
$C_s$			Stray capacitance (general); capacitance from negative summing point to common
$C_{STD}$			Standard capacitance or capacitor
$CME$	Common-mode error	Volts	The effective offset voltage appearing between the amplifier input terminals as a consequence of the voltage level of the positive input (Common-mode voltage)
$CMRR$	Common-mode rejection ratio		$\frac{ CMV }{ CME }$
$CMR$		Decibels	The logarithmic form of $CMRR$ . $CMR = 20 \log_{10} CMRR$
$CMV$	Common-mode voltage	Volts	See Nomenclature
$D$	Diode		
$E$	Voltage	Volts	DC reference voltage level, or effective reference voltage level
$E_B$			Power supply or zener diode breakdown voltage
$E_b$			Power supply or battery
$E_{bb}$			Battery terminal voltage
$E_{in}$			DC input signal level
$E_n, E_0$	Voltage, constant	Volts	DC null (or error) voltage

SYMBOL	TERM	UNITS	EXPLANATION
$E_R$			Generally, the voltage across a resistor
$E_r, E_{REF}$			Reference or bias
$E_{RESET}$			Level at which an initial condition is set
$E_s$			Generally, the reference level around which a signal varies
$E_Z$			Voltage across a Zener diode
$e$	Signal voltage	Volts	Output of operational circuit. Rarely $e_o$ (never $e_0$ ) in Philbrick Literature
$e_0, e_1, e_2$			Input signal, also $e_{in}, e_s$
$e_A, e_B$			Signal voltages at points A and B in a circuit (to ground)
$e_g$			Signal generator output voltage Gate logic input
$e_i, e_j$			Two signal voltages in a numbered series
$e_{LG}$			AC signal voltage introduced by power line coupling to or from ground (see I.28)
$e_N$			Noise voltage source
$e_n$			Null voltage of an Operational Amplifier (error voltage)
$f$	Frequency	Hertz (cps)	
$f_H$	Frequency, high		The frequency at which amplifier open-loop gain is unity gain-bandwidth product product (see also $\omega_H$ )
$G$	Conductance	mho, $\bar{u}$	
HQG	High Quality Ground		Signal ground; reference for lowest-level signal in the system (as opposed to chassis ground, earth, or power common)
$I$	DC current	Ampere	



SYMBOL	TERM	UNITS	EXPLANATION
$I_A, I_B$	Current	(Amperes)	Bias or reference current into or out of amplifier input terminal
$I_o$			Offset current
$I_{oA}, I_{oB}$			Offset currents associated with amplifier input terminals
$I_{ss}$			Idling current or steady-state component of current
$i$			Signal current; also the dynamic component of current; usually with identifying subscripts
$i_D$			Diode current
$i_{in}$			Input current
$i_L$			Load current
$i_M, I_M$			Meter current
$i_{NA}, i_{NB}$			Noise current associated with amplifier input terminals
$i_s$			Signal current
$j$	$\sqrt{-1}$		Imaginary term operator in a complex expression (mathematical "i")
$K, k$	Arbitrary constants		(Often with subscripts)
$k$	Boltzmann's Constant	Joule degree K	$1.38054 \times 10^{-23}$
$M$	Meter		
$P$	Potentiometer		
$p$	Heaviside operator	$\text{sec}^{-1}$	$py \equiv \frac{dy}{dt}, \frac{1}{p}y = \int ydt$
$Q$	Quality factor		Of a circuit or component; specifically the ratio of energy storage to energy dissipation therein. ( $Q = \frac{1}{2}\zeta$ ) Also, charge (i.e., on a capacitor) (coulombs)
$q$	Charge	Coulomb	For example, charge of an electron
$R$	Resistance, resistor	ohms $\Omega$	Usually with identifying subscripts
$R_A, R_B$			Input resistance, terminal A, terminal B to power common
$R_{AB}$			Input resistance, terminal A to terminal B
$R_{be}$			Base-emitter resistance of a transistor (sometimes $r_{be}$ )
$R_i$			Internal resistance, of an Operational Amplifier output circuit
$R_{in}$			Input circuit resistance or resistor
$R_L$			Resistive component of load
$R_m$			Meter resistance
$R_s$			Source resistance
$R_{STD}$			Standard (or reference) resistance or resistor
$R_x$			Unknown resistor or resistor to be measured

SYMBOL	TERM	UNITS	EXPLANATION
$S$	Switch		
$T$	Absolute temperature Time Constant RC	Degrees K Seconds	Sometimes $\theta$ ( $^{\circ}\text{C}$ )
$t$	Time	Seconds	
$V$	Voltmeter		
$V, v$	Voltage	Volts	(See also $E$ or $e$ )
$V_o$			Offset voltage
$V_{oB}$			Offset voltage between amplifier input terminals
$V_d$			Junction voltage drop
$V_f, v_f$			Diode forward drop
$X_c$	Capacitive reactance	ohms $\Omega$	
$Y$	Admittance	mhos $\mathfrak{U}$	The inverse of impedance, $Y = G + jB$ (for continuous sine waves)
$Z$	Impedance	ohms $\Omega$	$Z = R + jX$ (for continuous sine waves)
$Z_A, Z_B$			Input impedance, terminal A to ground, terminal B to ground
$Z_{AB}$			Input impedance, terminal A to terminal B
$Z_{AG}, Z_{BG}$			Input impedance to ground, same as $Z_A, Z_B$
$Z_f$			Generally, feedback impedance
$Z_{in}$			Generally, input impedance
$Z_L$			Load impedance
$Z_{REF}$			Reference impedance or $Z_{STD}$ , Standard impedance
$Z_{\omega_0}$			Impedance at $\omega_0$ i.e., at center frequency
$\alpha$	Noise components, resistance ratio		
$\beta$	Feedback divider ratio Transistor current gain		Complex attenuation of feedback paths
$\Delta e, \delta e$	Null or error voltage		
$\epsilon$	Base of natural logarithms		
$\theta$	Phase angle	Degrees or radians	
$\Phi$	Philbrick		Leadership in feedback technology
$\rho$	Ratio		Fractional rotation of a potentiometer or rheostat
$\tau$	Time interval, or time constant		
$\phi$	Phase, phase shift		Also angle of phase shift
$\omega$	Angular frequency	Radians/sec	$\equiv 2\pi f$
$\omega_C$	Critical frequency		Or cutoff frequency: $\omega_{CU}$ and $\omega_{CL}$ are upper and lower cutoff frequencies
$\omega_H$	Upper radian frequency		$2\pi f_H$ see $f_H$
$\omega_0$	Center frequency		$\omega_0 = \sqrt{\omega_{CU} \omega_{CL}}$

# BIBLIOGRAPHY

The Analog Art and the Operational Amplifier are inseparable, having common roots in feedback; and both have been sources of fascination to us during the past twenty years and more. Although the Operational Amplifier seems destined for a grand future as a component in instrumentation and "building-block" electronics, one can always find refreshment, inspiration, and guidance at the Source. As an example, we list here an incomplete sampling of the books to be found—in our library, but—in our offices and laboratories, and, opened, on the desks of our engineers. Please note the rather heavy emphasis on Analoguery.

Following that list is one of articles and publications printed or reprinted by us in recent years and still available at no charge, arranged by subject. For a more comprehensive (though somewhat dated) list, see *The Lightning Empiricist*, Volume 12, Number 2, April, 1964. Admittedly, even these are but a drop in the ocean of literature that has been and (especially) is yet to be written on this subject.

For those who would dig even more deeply, we suggest reference to the applications publications of companies that manufacture analog products. Readers of this Publication are of course invited to keep up to

date via the Philbrick mailing list. Among these, one should consider the continuing evolution of our own *Applications Briefs*, *The Lightning Empiricist*, new reprints, technical data, and catalog documentation. We also recommend to our readers the splendid service, now performed by Simulation Councils, Inc., of La Jolla, California, in their journal, *Simulation*, entitled "Simulation Survey and Literature Review," formerly published at the Georgia Institute of Technology as *Analog Computers Literature Review*, by Mr. L. W. Ross.

## BOOKS

<i>Analog Computation</i>	Jackson	McGraw-Hill
<i>Analog Computing in Engineering Design</i>	Rogers & Connolly	McGraw-Hill
<i>Analog Simulation</i>	Karplus	McGraw-Hill
<i>Analogue and Digital Computer Methods in Engineering Analysis</i>	James, Smith, & Welford	International Text-book Company
<i>Analogue Computation (4 Vols.)</i>	Fifer	McGraw-Hill
<i>Analogue Computers (Translated from the Russian)</i>	Eterman	Pergamon Press
<i>Analogue Computing at Ultra High Speed</i>	MacKay & Fisher	Wiley
<i>Computer Handbook</i>	Huskey & Korn	McGraw-Hill
<i>Computers in Education</i>	Hall	Pergamon Press
<i>Design Fundamentals of Analog Computer Components</i>	Howe	D. Van Nostrand Co.
<i>Electronic Analog and Hybrid Computers</i>	Korn & Korn	McGraw-Hill
<i>Electronics for Scientists</i>	Malmstadt, Enke, & Toren	W. A. Benjamin, Inc.

### *Elektronischer Analogrechner*

*Experiments in Electronics*  
*Generalized Instrumentation for Research and Teaching*

Ernst	R. Oldenbourg, Munich
Evans	Prentice-Hall
Morrison	Washington State U. Press (re-printed by and available gratis from Philbrick Researches)
Grabbe, Ramo, Wooldridge (Editors)	Wiley
Tomovic & Karplus	Wiley
Ashley	Wiley
Warfield	Prentice-Hall
Harris	Wiley
Murray	Columbia U. Press
Paynter	Philbrick Researches

### *Handbook of Computers and Control*

### *High Speed Analog Computers*

*Introduction to Analog Computation*  
*Introduction to Electronic Analog Computers*

### *Introduction to Feedback Systems*

### *Mathematical Machines (Vol. 2)*

### *A Palimpsest on the Electronic Analog Art*

## REPRINTS & ARTICLES

### I. APPLICATIONS

#### A. Bio-Medical Analysis

"Analog Computation of Respiratory Response Curve" T. W. Murphy, Memorial Sloan-Kettering Cancer Center, and R. Crane, Electronic Gear, Inc. (Reprint No. 41)

"A New Instrument For The Summation Of Evoked Responses From The Nervous System" Burton S. Rosner, Ph.D., Truett Allison, M.A., Elliot Swanson, B.S.E.E., and William R. Goff, Ph.D., West Haven Veterans Administration Hospital, Yale University School of Medicine, and Ampex Corporation. (Reprint No. 37)

"Respiratory Carbon Dioxide Response Curve Computer" J. Weldon Bellville, Sloan-Kettering Institute, and J. C. Seed, Wellcome Research Laboratory. (Reprint No. 26)

#### B. Computers

"Analog Techniques Applied To Business Models" F. M. Verzuh and P. D. Hansen. *The Lightning Empiricist* (XII:1).

"Analog Yesterday, Today & Tomorrow" G. A. Philbrick. *The Lightning Empiricist* (XI:4).

"Automatic Digital Setup and Scaling of Analog Computers" Dr. Henry M. Paynter, Massachusetts Institute of Technology, and Julian Suez, International Business Machines Corporation. (Reprint No. 47)

"Intentionally Unconventional Analoguery" *The Lightning Empiricist* (XI:1).

"Matrix Programming Of Electronic Analog Computers" R. E. Horn, Westinghouse Electric Corporation, and P. M. Honnell, Washington University. (Reprint No. 2)

"Modern Analog Computing Machines" G. A. Philbrick, Philbrick Researches, Inc.

"A New Active-Passive Network Simulator For Transient Field Problems" Walter J. Karplus, Dept. of Engineering, University of California. (Reprint No. 31)

"Precision Analog Memory Has Extended Frequency Response" T. A. Brubaker, Dept. of Electrical Engineering, University of Arizona. (Reprint No. 36)

"A Report To Engineers And Management" George A. Philbrick Researches, Inc. (Reprint No. 24)

"Ordering and Selection Processes and Ultra-Reliable Systems" H. M. Paynter, Massachusetts Institute of Technology.

"Time Domain Synthesis Based On A Passive Tardigrade Module" *The Lightning Empiricist* (XI:3).

#### C. Industrial Process Analysis

"Operational Amplifier Techniques in Process Control" Dr. Peter D. Hansen, Philbrick Researches, Inc. (Reprint No. 45)



"Computer Representations of Engineering Systems Involving Fluid Transients" F. D. Ezekiel, Massachusetts Institute of Technology, and H. M. Paynter, Massachusetts Institute of Technology. (Reprint No. 12)

"Contribution to the Stability Theory of Systems of Surge Tanks" Charles Jaeger, Water Turbine Dept., English Electric Company Limited. (Reprint No. 3)

"Dynamic Analysis of Heat Exchanger Control" Bruce D. Hainsworth, The Foxboro Company, Vincent V. Tivy, The Foxboro Company, and Dr. Henry M. Paynter, Massachusetts Institute of Technology. (Reprint No. 1)

"Fast Time Scale Simulation of a Reactor Control System" G. Friedensohn, Nuclear Dev. Corp. of America, and D. H. Sheingold, Philbrick Researches, Inc. (Reprint No. 11)

"Hydraulics by Analog" Henry M. Paynter, Massachusetts Institute of Technology. (Reprint No. 8)

"On an Analogy Between Stochastic Processes and Monotone Dynamic Systems" H. M. Paynter, M.I.T. (Reprint No. 5)

#### D. Instrumentation

"Capabilities of Some Non-Linear Instrument Circuits for Low-Level Transients" Bruce Seddon, Philbrick Researches, Inc. (Reprint No. 40)

"Vacuum Tube Electrometers Using Operational Amplifiers" G. F. Vanderschmidt, Lion Research Corporation. (Reprint No. 30)

"Subaudio Tunable Amplifier" J. M. Reece, Naval Research Lab. (Reprint No. 29)

"Operational Amplifier as Direct-Reading Precision Resistance Comparator" Philbrick Researches, Inc. Application Brief.

"P65A's Used to Form a Low-Noise Differential Instrument Amplifier" Philbrick Researches, Inc. Application Brief.

"A Precision Amplitude-Distribution Amplifier" W. F. Caldwell, G. A. Korn, V. R. Latorre, and G. R. Peterson, Dept. of Elec. Engrg., University of Arizona. (Reprint No. 28)

"Instrumentation Based on Operational Amplifiers" (Parts I & II). C. N. Reilley, University of North Carolina. (Reprint No. 42)

"Controlled-Potential and Derivative Polarograph" and "Controlled-Potential Polarographic Polarizing Unit with Electronic Scan and Linear Residual Current Compensation" M. T. Kelley, H. C. Jones, and D. J. Fisher, Oak Ridge National Laboratory. (Reprint No. 25)

"Electronic Analog Instruments As Tools of Research & Development" George A. Philbrick, Philbrick Researches, Inc. (Reprint No. 35)

"Electronic Controlled-Potential Coulometric Titrator" M. T. Kelley, H. C. Jones, and D. J. Fisher, Oak Ridge National Laboratory. (Reprint No. 20)

"Electronic Determination of the I, G, and I/G Parameters of a Tunnel Diode" C. R. Gneiting, The Johns Hopkins University, Radiation Laboratory. (Reprint No. 34)

"Incremental Approach to Derivative Polarography" Clemens Auerbach, H. L. Finston, George Kissel, and Joseph Glickstein, Brookhaven National Laboratory. "Stationary Electrode Polarography with a Staircase Voltage Sweep". Charles K. Mann, Florida State University. (Reprint No. 38)

#### "Operational Amplifiers Symposium"

"Generalized Circuits for Electroanalytical Instrumentation" W. M. Schwarz and Irving Shain, University of Wisconsin.

"A Multipurpose Operational Amplifier Instrument for Electroanalytical Studies" William L. Underkofler and Irving Shain, University of Wisconsin.

"Power of Time and Exponential Current Chronopotentiometry" Royce W. Murray, University of North Carolina.

"A Multipurpose Electromechanical Instrument for Control of Potential or Current" George Lauer, Helmar Schlein, and R. A. Osteryoung, North American Aviation Science Center.

"Electroanalytical Controlled-Potential Instrumentation" Glenn L. Booman and Wayne B. Holbrook, Phillips Petroleum Co., Atomic Energy Division.

"A Digital Readout Device for Analog Integrators" E. Clifford Toren, Jr., and Charles P. Driscoll, Duke University.

"A. C. Polarography Employing Operational Amplifier Instrumentation" Donald E. Smith, Northwestern University.

"A Practical Instrument Synthesizer" Charles F. Morrison, Washington State University.

"The Heath Analog Computer as a Versatile Analytical Tool" Galen W. Ewing, New Mexico Highlands University, and Thomas H. Brayden, Jr., Louisiana State University.

"Instrumentation for Cyclic and Step-Function Voltammetry Using Operational Amplifier Switching Modules" Richard P. Buck and Robert W. Eldridge, Bell & Howell Research Center.

(Reprint No. 43)

"Recording Optical Pyrometer" Norman A. Blum, Avco Manufacturing Corporation. (Reprint No. 17)

"Second Harmonic Alternating Current Polarography with a Reversible Electrode Process" D. E. Smith and W. H. Reinmuth, Columbia University. (Reprint No. 33)

#### E. Signal Conditioners

"Impedance & Admittance Transformations" D. H. Sheingold. *The Lightning Empiricist* (XII:1).

"Missile Rate Simulator Provides Sinusoidal Motion for Guidance Systems" Joel K. Nelson, Boeing Airplane Co. (Reprint No. 16)

"A Particular Application of FM Tape Used With An Analogue Computer" David J. Cholley, Hercules Powder Company. (Reprint No. 39)

## II. CIRCUIT TECHNIQUES

### A. Computer Techniques

"A Circuit With Logarithmic Transfer Response Over 9 Decades" J. F. Gibbons and H. S. Horn, Stanford University. (Reprint No. 49)

"Multiplication and Logarithmic Conversion By Operational Amplifier-Transistor Circuits" William L. Pateron, Litton Industries. (Reprint No. 46)

"New Integrating Circuit and Electronic Analog for Transient Diffusion and Flow" J. Ross MacDonald, Texas Instruments, Inc. (Reprint No. 14)

"Q3-M1P Multiplier" *The Lightning Empiricist* (XII:3-4).

"Rate-of-Change Indicator" *The Lightning Empiricist* (XI:4).

### B. Fundamental Circuit Techniques

"Analog Methods" Bruce Seddon, Philbrick Researches, Inc. (Reprint No. 27)

"Analog Computer Techniques Applied To Industrial Instrumentation and Control" George A. Philbrick Researches, Inc. (Reprint No. 18)

"Operation Of The USA-3 Amplifier With Positive Open-Loop Polarity" Philbrick Researches, Inc. Application Brief.

"PP65 As Amplifier With High Input Impedance" Philbrick Researches, Inc. Application Brief.

"Single-Ended Inverted Amplifiers" Philbrick Researches, Inc. Application Brief.

"Stabilized Follower Amplifier" Prof. Donald Deford, Northwestern University. (Reprint No. 23)

"Typical Operational Amplifier Applications" D. H. Sheingold, Philbrick Researches, Inc.

### C. Voltage Current Regulation

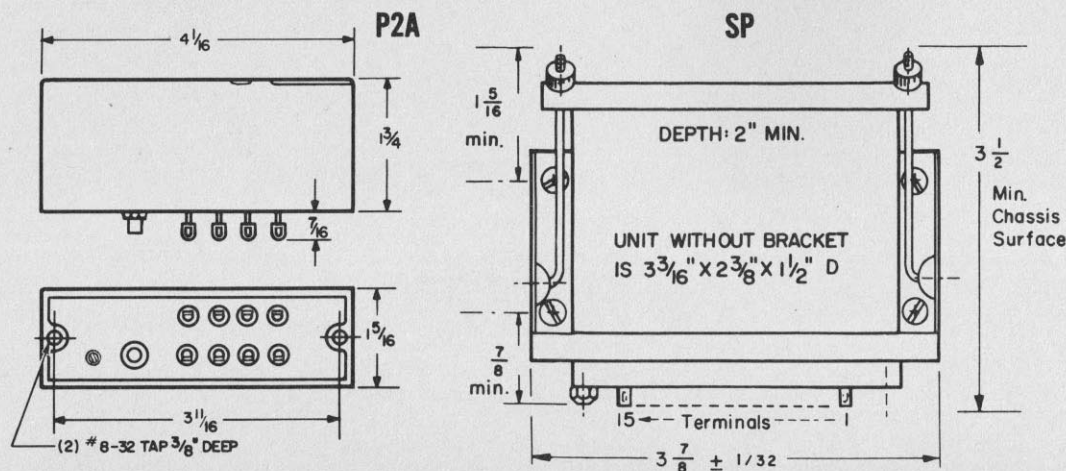
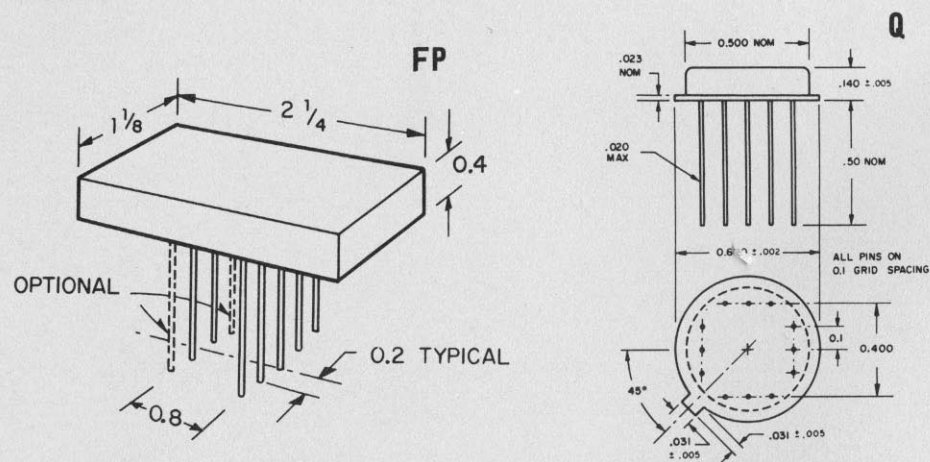
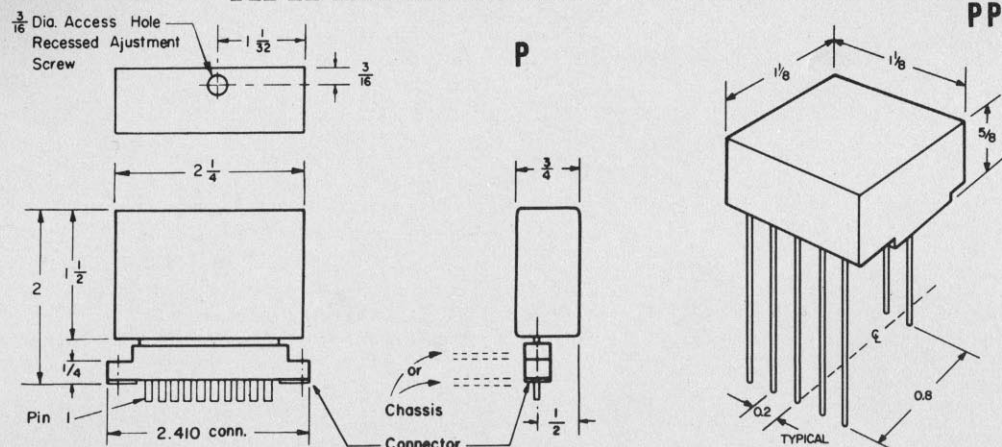
"Analog Computer Reference Supply" C. E. Foiles, J. P. Hartmann, and H. Koerner, University of Arizona. (Reprint No. 21)

"High Precision Large Current Regulator" K. C. Brog and F. J. Milford, Case Institute of Technology. (Reprint No. 32)

"Operational Amplifier As Constant Current Source—I" Philbrick Researches, Inc. Application Brief.

"Use of Operational Amplifiers in Precision Current Regulators and Use of Operational Amplifiers in Accelerator Beam Control Systems" Karl Eklund, Columbia University. (Reprint No. 22)

# AMPLIFIER DIMENSIONS



Philbrick Utility-Grade Amplifiers, identified by the letter "U" following the family number (e.g. P65AU), are identical to premium-grade prototypes in circuitry, layout, manufacturing techniques, and the exclusive use of silicon transistors and first-grade passive components from leading U. S. manufacturers. The price difference is achieved by the following means:

The use of silicon transistors encapsulated in highly moisture-resistant silicone plastic (Note: not epoxy!) instead of hermetically-sealed amplifiers.

Use of capacitors which are guaranteed from  $-55$  to  $+85^{\circ}\text{C}$ , instead of the  $-65$  to  $+125^{\circ}\text{C}$  units normally used in premium units.

All room-temperature tests are carried out with the thoroughness that has earned Philbrick an enviable reputation for reliability; **complete** temperature tests are run on representative samples of each production run to confirm compliance with published specifications.

Use of date codes and go-no-go tests instead of serial numbers and recording of data as normally required for all premium units (Government Inspection and/or certified test results are always available, upon request, for **premium** units.)

In performance, the Utility-Grade amplifiers are within their operating temperature range identical to their Premium-Grade counterparts. As low-temperature tests are conducted on samples only, gain tolerances are relaxed by a factor of 2, and the input current vs. temperature tolerances by a factor of 1.5, compared with the corresponding specifications for the premium amplifier.

Philbrick Utility-Grade amplifiers may be substituted in virtually all applications for which Premium-Grade counterparts are recommended.

Philbrick differential operational amplifier families P35 through P85 contain input stages with matched pairs of junction transistors in a common emitter configuration. Emitter current being kept constant, each transistor requires a "housekeeping" current into its base amounting to emitter current divided by  $\beta$  (current gain). By selecting high- $\beta$  transistors and low emitter currents, these base currents can be made as small as  $10^{-8}$  amperes, but they can never be eliminated, and they increase as temperature decreases. If the base currents of input transistors are not supplied by current sources within the amplifier, an output voltage error will result because this offset current produces a voltage drop across the feed-back impedance (in an inverter) or the signal source impedance (in a voltage follower).

The simplest form of base current supply is a resistor from  $+B$  to each base. P45A, P55A, P65A and P85A families have these built in, while the proper resistance values for external installation are marked on their PP equivalents. Although these current trim resistors are inexpensive, they are most effective within narrow temperature limits and where high common-mode voltages do not occur. After all,  $\beta$ , and with it base current do change with temperature, and a resistor is a constant current source only as long as the voltage across it remains constant!

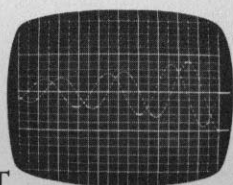
Philbrick Current Compensated Amplifiers, identified by the letter C following the family number, have built-in base current sources which closely track current demand over the entire operating temperature range.

The P35C and P85C series contain a sophisticated compensating circuit which leaves the outstanding common mode voltage rejection ratio, the common mode voltage range, and the input impedances unaffected. An additional feature of this compensating circuit is a provision for nulling either input current completely by applying an adjustable voltage bias ( $\pm 5$  volts maximum) to a terminal provided for the purpose. The P45C and P65C series contain a simpler compensating circuit which provides a fivefold decrease in offset current over the entire temperature range, but also reduces the common mode rejection ratio, the common mode voltage range, and the input impedance.



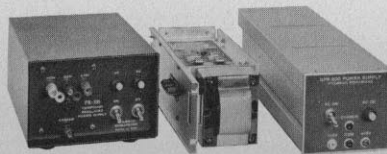
# PHILBRICK PRODUCTS & SERVICES FOR SCIENCE & INDUSTRY

## MULTI-CHANNEL CALIBRATED DISPLAY SYSTEM for ANALOG COMPUTOR READOUT



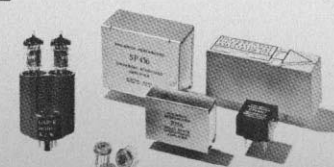
A convenient monitor of related variables for analog computing, dynamic testing, and laboratory experiments ... This versatile, easy-to-use, and precise oscilloscopic readout instrument will display up to eight separate functions simultaneously in correct absolute time and phase relationship, on an electronically produced and displayed, accurately-set coordinate system, for quick, graph-paper readout of time and voltage.

## SYSTEM & INSTRUMENT POWER SUPPLIES



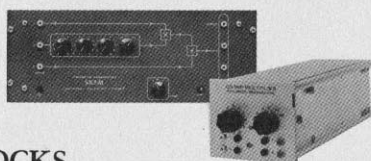
Available in rack, cabinet, modular, plug-in, or build-in form, Philbrick power supplies are precisely regulated and essentially noise-free—typically, regulation (including drift) is of the order of 100 PPM, noise and hum less than 1 PPM, and recovery (to within .001%) from a step-change in load is accomplished in a few microseconds. Standard ratings are compatible with Philbrick (and many other) amplifiers and systems.

## OPERATIONAL AMPLIFIERS FOR EVERY NEED



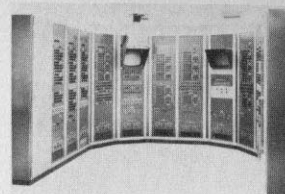
By early 1965, we had shipped approximately 300,000 Philbrick operational amplifiers, the great majority of which are still in frequent if not continuous use. The Philbrick line embraces every major type of operational activator and instrumentation amplifier, in a dozen different forms and in literally hundreds of standard variations.

## COMPUTOR & SYSTEM BUILDING BLOCKS



Philbrick equipment for the implementation of both analog and hybrid computers, simulators, and analyzers, includes: arbitrary function generators, universal linear operators, multiplier-dividers, and manifolds of several kinds, (See also the Q3 packaging system, elsewhere on this page.)

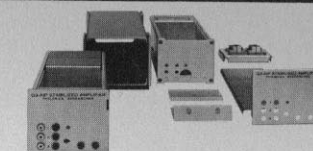
## COMPUTATION/ SIMULATION SERVICES & FACILITIES.



Our goal remains unchanged over the years: to marry operational concepts with electronic technology in pioneering new instruments and computing systems. Toward this end, we solicit and welcome the opportunity to consult with you, without charge.

Consulting services on a more formal, fee basis are available at our computing center in Dedham, Mass.

## THE Q3 MODULAR PACKAGING SYSTEM



We consider this purely mechanical development to be one of our most important recent contributions to the electronic art. It employs as its modulus an extruded outside shell 4.2" w x 3.5" h x 13" l, into which the modular chassis slides on four rails. These shells may be used individually or permanently joined together both vertically and horizontally to form a matrix of rectangular cells that will stack in locking fashion without being fastened together. Standard front panels, modular chassis, adaptors, and accessories are available.

## DOING BUSINESS WITH PHILBRICK ...

It is our pleasure to provide sympathetic attention, sound advice, interdisciplinary empathy, and economical implementation, in response to every serious enquiry. You may gain access to this low-pressure data interface through any of the channels listed at the right.

If either the intensity or the magnitude of your problems justifies formal contact with our Applications Engineering staff, you will find us most receptive to marathon telephone conferences. Those whose corporate policy and limited budget prohibit the use of long distance are welcome to phone collect. You are, of course, always welcome at our beautiful new Dedham facility.

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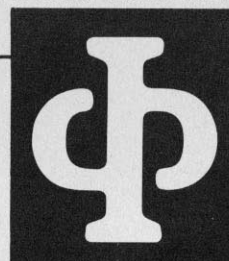
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# INDEX

## A

Absolute-Value Circuit	59
Precision (II.42)	59
Simple (II.42)	59
AC Average Reader, Precise (III.54)	89
AC Integrator (III.73)	98
AC Millivoltmeter, Precise (III.55)	90
AC Noise Components (I.9)	14
Adder (II.3)	41
Inverting (II.36)	57
Inverting, Weighting of (II.3)	41
Non-Inverting (II.4)	41
Adder-Subtractor (II.5)	42
Adjustable-Coefficient Circuit, Bipolar (II.7)	43
Adjustable-Coefficient Inverters (II.6)	42
Adjustable Lag — Non-Inverting,	
Inverting (II.16)	47
Adjustable-Scale Combiner, Bipolar (II.8)	43
Admittance, Negative (III.71)	97
Amplifier	31
Activator (I.40)	31
Booster (I.44)	33
(I.45)	34
Bridge (III.80)	102
Broadband (I.18)	19
"Charge" (III.41)	83
Chopper Stabilized (I.12)	15
Commercial, Performance Classes (I.37)	30
Commercial, Packages (I.38)	30
Current, Low-Noise,	
Gain of 1,000,000,000 (III.38)	82
DC Precision (III.29)	79
Demodulator (III.69)	96
Differential-Input	
Very-High-Impedance (I.4)	11
(III.39)	82
Differential, Current	
for Photomultipliers (III.40)	83
Differential Input (I.4)	11
Electronic (I.2)	10
Functional Description of (I.3)	10
Gated (II.48)	61
(II.51)	62
Input Configuration (I.4)	11
Null, Logarithmic Response (III.45)	85
Operational (I.1)	10
Operational in HV Follower (III.34)	80
Operation, Imperfections (I.7)	13
Precision DC (III.29)	79
Current, Photomultiplier-Differential (III.40)	83
Precise (1 PPM) "DC" (III.29)	79
"Saturated" (I.25)	23
Schematic Symbol (I.3)	10
Solid-State Electrometer (III.36)	81
Stabilizing (I.12)	15
Single Ended (I.4)	11
Wideband (1000 gain) (III.42)	84
Amplitude-Limiter Circuits	
for signal generators (III.10–III.15)	68–71
Arbitrary-Function Fitter (II.26)	52
Averager, Weighted (II.9)	43

## B

Backlash, Simulation of (II.45)	60
Band-Pass Filters (III.27)	77
Band-Reject Filters (III.27)	77
Bandwidth, Limited (I.18)	19
Bias Circuits	
Temperature-Compensating (I.22)	21
Internal Voltage and Current (I.21)	21

## Bias

External Voltage (I.19)	20
External Current (I.20)	20
Follower (I.23)	22
Biasing, Offset and (I.8)	14
Bipolar Adjustable-Coefficient Circuit (II.7)	43
Bipolar Adjustable-Scale Combiner (II.8)	43
Bistable Multivibrator (III.20)	73
Booster Amplifier	
Emitter Follower (I.45)	34
High Efficiency (I.46)	34
Need for (I.43)	33
Bound Circuits (I.25)	23
Bounds, Low Leakage (I.25)	23
Bridge Amplifiers (III.80)	102
Bridge, Capacitor,	
Precise Integrator Type (III.48)	87
Bridge, Kelvin (III.44)	85

## C

Capacitance, Input, Neutralizing	
(in Follower w/Gain) (III.37)	81
Capacitance Multiplier (III.72)	98
Capacitor Deviation Bridge, Precise (III.48)	87
Capacitor	
Characteristics and Types (I.33)	27
Compensating (I.18)	19
(I.42)	32
Polystyrene (I.33)	27
Cathode Follower (for VT Circuit) (III.34)	80
CRO in Measurement of Open-Loop Gain (I.47)	35
"Charge" Amplifier (III.41)	83
Chassis Ground (I.30)	26
Choppers, Bounce	
Closure Synchronization	
Dwell Time	
Mechanical Lag	
(I.36)	29
Circuit, Bound (I.25)	23
Circuit Performance, Ideal (I.6)	12
Clipper (II.43)	59
"Clipping" of Output	
in Square Wave Generator (III.18)	72
Closed-Loop Gain and Open-Loop Gain (I.41)	31
Closed-Loop Relationship, Ideal (I.6)	12
Coefficient Circuit, Bipolar Adjustable (II.7)	43
Common-Mode Error (I.16)	17
Common-Mode Error, Measured (I.48)	36
Common-Mode Rejection Ratio	
(CMRR) (CMR) (I.16)	17
(I.48)	36
Comparator, Precision (III.78)	101
(II.41)	58
Conformal Transformation of Filters (III.26)	76
(III.28)	78
Constant-Current Regulator (III.9)	68
Controller with Independent Adjustments	
(III.77)	100
Converter, Charge-to-Voltage (III.41)	83
Current Amplifier, Low Noise (III.38)	82
Current Bias	
Internal (I.21)	21
Simple (I.20)	20
Current, "Idling," in Boosters (I.46)	34
Current Measurement (III.30)	79
Current Measurement Picoampere Levels	
(III.59)	91
Current Offset (I.7)	13
Current Offset Biasing	
in S.S. Electrometer (III.36)	81
Current Pump I, Floating Load (III.3)	65
Current Pump II	
Floating Load (III.4)	65
Grounded Load (III.5)	66
Current Pump IV	
Grounded Source and Load (III.6)	66
Current Pump V, Chopper Stabilized (III.7)	67
Current Pump, Single Transistor (III.8)	67
Current-to-Voltage Transducer (III.30)	79

## D

Damping Circuit in Sine Wave Oscillator	
(III.10)	68
Dead Zone (II.44)	59
Delay-Line Element (II.18)	47
Demodulator-Amplifier (III.69)	96
Derivation Approach, for Error Factor (I.15)	16
Derivative dy/dx from Time Derivatives (III.68)	95
Deviation Measurement, Kelvin Bridge (III.44)	85
Deviation Measurement Wheatstone Bridge	
(III.43)	84
Difference Integrator (II.13)	46
Differential Amplifier,	
Very-High-Impedance (III.39)	82
Differential-Current Amplifier,	
Photomultiplier (III.40)	83
Differential-to-Single-Ended Transition (III.39)	82
Differentiator (II.19)	48
Augmenting (II.20)	48
Long Term (III.56)	90
Diode-Transistor Leakage Measurement (III.60)	92
Diodes, Transistors, Automatic	
Testing and Sorting (III.60)	92
DC Amplifier	
Wideband Gain of 1000 (III.42)	82
Precision (III.29)	79
DC Beta, Measurement of (III.59)	36
DC Offsets, Measurement of (I.49)	46
Double Integrator (II.14)	15
Drift (I.11)	15
Methods of Minimizing (I.12)	29
"Dry" Circuit Resistance (of Contacts) (I.36)	29
Dual Mode Circuit	
Simple (Inverting) (II.36)	57
Simple (Non-Inverting) (II.37)	57
Dynamic Stability, Achievement of (I.42)	32

## E

Electrometer Amplifier, Solid-State (III.36)	81
Electrometer-Millivoltmeter Amplifier (III.61)	92
Electronic Switch (II.40)	58
Electrostatic Shield (I.31)	26
Emitter-Follower Booster (I.45)	34
Emitter-Followers (III.8)	67
"End-Resistance Offset" of Potentiometers	
(I.35)	29
Environment, Effects of (I.13)	16
Error, Common Mode (I.16)	17
Error Factor, Finite-Gain (I.15)	16

## F

Fault Currents (I.27)	24
Fault Protection (I.27)	24
Feedback (I.6)	12
Positive, in Signal Generators	
(III.10–III.21)	68–74
Feedback Network	
3-Terminal (Tee) (I.26)	24
Activation of (I.40)	31
Filters	
Active (III.22–III.28)	74–78
"Averaging" (III.25)	76
Cascaded (III.24)	75
Nomenclature and Symbolology (III.22)	74
Finite-Gain Error Factor (I.15)	16
Fixed Voltage Precise Reference (III.1)	64
Flicker (I.10)	14
Measurement (I.50)	37
"Flip-Flop" (III.20)	73
Follower (II.2)	40
Chopper Stabilized (Switched Operation)	
(III.33)	80
Precision High-Voltage (III.34)	80
Simple (III.32)	80
Simple — Dual Mode (II.37)	57
Follower-with-Gain (II.2)	40
Four-Quadrant Multiplier (II.32)	55

Frequency Measurement (III.66)	94
(III.67)	95

## Function

Anti-Log (II.28)	53
(II.30)	54
Arbitrary (II.26)	52
Log (II.22)	50
(II.24)	52
Function	
Sine (or Cosine) (II.27)	53
Squaring (II.25)	52
Function Generation, by Piecewise	
Linear Networks (II.23)	51

## G

Gain (I.15)	16
Closed Loop (I.41)	31
Loop (Inverse Attenuation) (I.41)	31
Measurement of Open Loop (I.47)	35
Open-Loop, Performance Limitations (I.6)	12
Roll-Off with Frequency (I.17)	18
Gain-Bandwidth Product (I.17)	18
Gain of 1000 Amplifier, Wideband (III.42)	84
Gate, Precision (II.39)	58
Gated Amplifier (II.48)	61
(II.51)	62
Generator	
Sawtooth, Precise (III.16)	71
Sine-Cosine (2-Phase) (III.12)	69
Square-Wave, Simple (III.18)	72
Staircase (III.19)	73
Triangular-Wave, Precise (III.15)	71
Ground, Chassis, Power-Common, Signal	
(High Quality) (I.30)	26
Ground Conductors and Connections (I.30)	26
Grounding Philosophy (I.30)	26
Guard (I.31)	26
Guarding and Shielding Philosophy (I.31)	26

## H

"Hardware":	
Q3 Modular Electronic Package (I.39)	30
High-Quality Ground (HQG) (I.30)	26
"Hold" Performance of Track-Hold	
Memory (III.75)	99
"Howland Circuit" Current Pump (III.6)	66
Humidity (I.13)	16
Hysteresis, in Backlash Simulation (II.45)	60

## I

"Idling" Current (in High Efficiency	
Boosters) (I.46)	34
Impedance Admittance Circuits, Negative	
(III.71)	97
Impedance	
Infinite (in Current Pump) (III.6)	66
Negative (III.71)	97
Non-Linear (I.7)	13
Impedances in Unity-Gain Inverter (II.1)	40
Initial Conditions Reset (II.12)	45
(II.50)	62
(II.51)	62
Input Capacitance, Neutralizing of (III.37)	81
Input Impedances, Unbalanced (I.16)	17
Input, Chopper-Stabilized, Single-Ended (I.4)	11
Input Impedances (I.18)	19
Input-Output Limitations (I.7)	13
Inputs, Balanced, Differential (I.3)	10
Insulation Resistance, Teraohms to Ground,	
Measurements of (III.46)	85
Integrator	
"AC" (II.12)	15
(III.73)	98
Augmenting (II.11)	44
in Capacitance Measurement (III.48)	87
Difference (II.13)	46
Double (II.14)	46



Free Running (II.12) .....	45	Multiplier-Divider (Quarter Square) (II.32) .....	55	<b>R</b>	Stabilization with Reactive Loads (I.44) .....	33	
Long Term, Memory (III.57) .....	91	..... (II.33) .....	55	"Rate Limiting" (I.57) .....	37	Stabilizer (I.12) .....	15
Reset (by Gated Amplifier) (II.51) .....	62	Multivibrator		RF Pickup (I.13) .....	16	Staircase Generator (III.19) .....	73
Reset (to Initial Conditions) (II.50) .....	62	Astable (Free-Running) (III.17) .....	72	RFI Filter Bushings,		Stray Leakage — Resistive — Capacitance	
Reset (to Zero Volts) (II.49) .....	61	Bistable (III.20) .....	73	Use in Low-Level Circuits (III.62) .....	93	(I.31) .....	26
in Resistance Measurement (III.46) .....	86	Monostable (III.21) .....	74	Ratio Circuits, Log of (II.28) .....	53	Subtraction (II.5) .....	42
in Saw-Tooth Generator (III.16) .....	71	<b>N</b>		Reactive Loads — Amplifier Stabilization		Sum of the Squares, Square Root of (III.65) ..	94
Single-Input and Summing (II.10) .....	44	Negative Coefficients (II.5) .....	42	with (I.44) .....	33	Summing Integrator (II.10) .....	44
in Triangular Wave Generator (III.15) .....	71	Negative Impedance/Admittance Circuits		Readout, Peak		Summing Point (I.5) .....	11
in True RMS Value Measurement (III.63) .....	93	(III.71) .....	97	Simple — Memory (III.49) .....	87	Switch, Electronic (II.40) .....	58
in Wien Bridge Oscillator (III.14) .....	70	Noise		Precise — Memory (III.50) .....	88	<b>T</b>	
Inverters, Adjustable-Coefficient (II.6) .....	42	Classifications (I.9) .....	14	Readout, Peak-to-Peak		Tape Preamplifier (NAB), Low Noise (III.70) .....	96
..... (II.7) .....	43	External Influences (I.13) .....	16	Simple — Memory (III.51) .....	88	"Tardigrade" Operation (II.15) .....	46
Inverter, Unity Gain (II.1) .....	40	Parameters (I.10) .....	14	Precise — Memory (III.52) .....	89	Tee Networks (I.26) .....	24
Inverting Adder (II.3) .....	41	Voltage, Measuring of (I.50) .....	37	Readout, Precise AC Average (III.54) .....	89	Temperature Effects (on Amplifiers) (I.13) .....	16
<b>K</b>		Non-Linearities in Amplifiers (I.7) .....	13	Readout, True RMS Value (III.63) .....	93	Thermal EMF (I.36) .....	29
Kelvin Bridge-Deviation Measurement		Non-Linear Circuits (II.28-III.33) .....	53-55	Recovery Time-Constant (I.25) .....	23	Thermal Gradients (I.13) .....	16
(III.44) .....	85	Non-Linear Devices		Reference, Precise, Fixed-Voltage (III.1) .....	64	Thermal Transients (I.13) .....	16
<b>L</b>		Continuous Function (II.22) .....	50	Regulator, Constant Current (III.9) .....	68	Three-Phase Oscillator (III.13) .....	70
Lag, Simple (II.15) .....	16	Synthesized-Function (II.23) .....	51	Relays (I.36) .....	29	Time Delay (II.18) .....	47
Lag Circuits, Adjustable (II.16) .....	47	Null Amplifier, Logarithmic Response (III.45) ..	85	Relay Switching in Track Hold Memory (II.46) ..	60	Time Integral (II.10) .....	44
Lag-Lead Element (II.17) .....	47	Null Deviation with 3-Grade Sorting (III.58) ..	91	Reset, Zero-Volt (II.49) .....	61	Time Integral of Difference	
Leakage		<b>O</b>		Reset, Initial-Condition (II.50, II.51) .....	62	between Signals (II.13) .....	46
Across Relay Contacts (I.36) .....	29	Offset and Biasing (I.7) .....	13	Resistance, True RMS Value (III.78) .....	101	Total Input Uncertainty (I.14) .....	11
..... (II.49) .....	61	..... (I.8) .....	14	Resistance, Insulation (III.46) .....	86	Track-Hold Long-Term Memory (III.75) .....	99
..... (II.50) .....	62	Open-Loop Gain vs. Frequency (I.17) .....	18	Resistance Measurement		Track-Hold Memory	
Capacitive and Resistive, in Relays and		Open-Loop Gain, Measuring (I.47) .....	35	Grounded Sample (III.43) .....	84	Permanent (III.76) .....	100
Choppers (I.36) .....	29	Open Loop Set-up, Closing the Loop (I.41) .....	31	..... (III.47) .....	86	Electronic Switching (II.47) .....	60
Dormant-Mode, Zeners (I.25) .....	33	Oscillator		Kelvin Bridge (III.44) .....	85	Gated-Amplifier Switching (II.48) .....	61
Reverse, Diodes (I.25) .....	33	Sinewave — Twin-Tee (III.10) .....	68	Teraohms to Ground (III.46) .....	86	Relay Switching (II.46) .....	60
..... (I.32) .....	27	Sinewave — Wien-Bridge (III.11) .....	69	Wheatstone Bridge (III.43) .....	84	Track-Hold-Peak Reader (III.53) .....	89
Leakage Measurement, Diode-Transistor		..... (III.14) .....	70	Wide Range (III.47) .....	86	Transconductor, Dual Logarithmic (II.22) .....	50
(III.60) .....	92	Sinewave — Amplitude Controlled (III.14) ..	70	Resistance, Negative (III.71) .....	97	Transducer	
Light Measurement, Low Level (III.40) .....	83	Three-Phase (III.13) .....	70	Resistors		Current-to-Voltage (III.30) .....	79
Linear "Combinor" (II.3) .....	41	Two-Phase (III.12) .....	69	in Adder/Subtractor (II.5) .....	42	Piezoelectric (III.41) .....	83
Loads, Active and Complex,		Overload Input, Recovery from (I.25) .....	23	in Zero Volt Reset (II.49) .....	61	Voltage-to-Current (III.31) .....	79
Current Pumps for (III.3-III.7) .....	65-67	<b>P</b>		Noise Generation in (I.34) .....	28	Transient Response, Measurement of (I.51) .....	37
..... (III.38) .....	82	Passive Network and Active Analog (I.1) .....	10	Types (I.34) .....	28	Transdiodes: Transistors Used as Diodes (II.22) ..	50
Log Multiplier (II.30) .....	54	Peak-and-Valley Measuring (II.48) .....	61	Response Equations		Transistor Parameter Measurement,	
..... (II.31) .....	54	Peak Reader and Memory		Ideal (I.5/6) .....	11	Picoampere Range (III.59) .....	91
Log of Ratio Circuits (II.28) .....	53	Simple (III.49) .....	87	Finite Gain (I.15) .....	16	Transition with Gain Carrier to DC (III.69) .....	96
Logarithmic Devices (II.22) .....	50	Precision (III.50) .....	88	RMS Value, True, Readout (III.63) .....	93	Transmission Delay (II.18) .....	47
Logarithmic Response (II.24) .....	52	..... (III.74) .....	99	Roll-Off, High and Low Frequency,		Triangular-Wave Generator, Precise (III.15) ..	71
Logarithmic Response Null Amplifier (III.45) ..	85	Peak Reader, Track-Hold (III.53) .....	89	AC and DC (I.12) .....	15	Triggering of Monostable Circuits (III.21) ..	74
Low Frequency Measurement		Memory, Simple (III.51) .....	88	"Roll-Off," Linear (I.1) .....	10	Triggering of Bistable Circuits (III.20) .....	73
and Conversion (III.67) .....	94	Memory, Precision (III.52) .....	89	Root Response (II.24) .....	52	True RMS Value Readout (III.63) .....	93
Low-Pass Filters (III.23) .....	75	Phase Characteristics, Measurement of (I.47) ..	35	<b>S</b>		Twin-Tee Oscillator (III.10) .....	68
Low-Noise Precision Preamplifier (III.35) .....	81	Phase Shift (I.17) .....	18	Saturation		<b>U</b>	
Low-Noise Precision Current Amplifier (III.38) ..	82	Phono Preamp (RIAA), Low Noise (III.70) ..	96	Positive and Negative (I.1) .....	10	Uncertainty, Input, Worst-Case (I.14) .....	11
<b>M</b>		Photomultiplier Differential Current		..... (I.25) .....	23	Unity-Gain Inverter (II.1) .....	40
Magnetic Field Measurement, Low Level (III.62)	93	Amplifier (III.40) .....	83	in Multivibrators (III.21) .....	74	<b>V</b>	
Memory		Polarity Separator (II.38) .....	57	Sawtooth Generator, Precise (III.16) .....	71	Voltage Bias	
Long-Term, Track-Hold (III.49-III.53) .....	87-89	Potentiometers (I.35) .....	29	Scaling for Differentiator (II.21) .....	49	External (I.19) .....	20
..... (III.74-III.76) .....	99, 100	Power Common Ground (I.30) .....	26	Scaling of Inputs (II.3) .....	41	Internal (I.21) .....	21
Peak Readout, Precise (III.50) .....	88	Power Supply, Floating (III.31) .....	26	Scaling for Integrator (II.10) .....	44	Voltage Bias (I.19-I.24) .....	20-22
..... (III.74) .....	99	Power Supply Philosophy (Regulation and Drift,		Selectors		Voltage Excursion (I.27) .....	24
Peak Readout, Simple (III.49) .....	87	Internal Impedance, Hum and Ripple) (I.29) ..	25	Compensated (II.35) .....	56	Voltage Measurement, AC (RMS) (III.63) .....	93
Peak-to-Peak Readout, Precise (III.52) .....	89	Preamplifier — Low Noise		..... (II.42) .....	59	Voltage Offset (I.7) .....	13
Peak-to-Peak Readout, Simple (III.51) .....	88	Precision (III.35) .....	81	Elementary (II.34) .....	56	Voltage Precise Reference, Fixed (III.1) .....	64
Permanent Track-Hold (III.76) .....	100	Tape or Phono (III.70) .....	96	Shielding and Guarding Phil. (I.31) .....	26	Voltage Source, Precision, Adjustable (III.2) ..	64
Track and Hold (Electronic Switch) (II.47) ..	61	Precise Voltage Source (III.2) .....	64	Signal Ground (I.30) .....	26	Voltage-to-Current Transducer (III.31) .....	79
Track and Hold (Gated Amplifier) (II.48) .....	61	Precision DC Amplifier (III.29) .....	79	Signal Source, Grounded (I.30) .....	26	<b>W</b>	
Track and Hold (Relay) (II.46) .....	60	Precision Gate (II.39) .....	58	Simple Lag (II.15) .....	46	Weighting Coefficients, in Inverting Adder (II.9)	43
<b>Meter/Converter</b>		Protection (I.27) .....	24	Sine-Cosine (2-Phase) Generator (III.12) .....	69	Wheatstone Bridge — Deviation Measurement	
High Frequency to DC (III.66) .....	94	<b>Q</b>		Sine-Wave Oscillator		(III.43) .....	84
Low Frequency to DC (III.67) .....	95	Q3 Modular Electronic Package (I.39) .....	30	Twin-Tee (III.10) .....	68	Wideband, High Gain Amplifier (III.42) .....	84
"Meter Relay," Meterless (III.79) .....	101	Q3 Series "U.O.M.'s" Operational		Wien-Bridge (III.11) .....	69	Wien Bridge Oscillator (III.11) .....	69
Millivoltmeter, AC (III.55) .....	90	Modules (I.39) .....	30	Wien-Bridge Amplitude Controlled (III.14) ..	70	..... (III.14) .....	70
Millivoltmeter-Amplifier, Electrometer		Quadratic Transconductor (II.23) .....	51	Slope-Symmetry Adjustment (Control) (III.15) ..	71	<b>Z</b>	
(III.61) .....	92	..... (II.25) .....	52	Squarer (II.25) .....	52	Zener Diode, Ideal (I.25) .....	23
Milliammeter, Zero-Drop (III.55) .....	90	Quarter-Square Divider (II.33) .....	55	Squarer, Odd-Value (III.64) .....	93	Zero-Drop Milliammeter (III.55) .....	90
Modulated-Carrier Used as "Chopper" (I.12) ..	15	Quarter-Square Multiplier (II.32) .....	55	Square Root Circuits (II.24) .....	52	"Zero-Drop" Shunt (III.55) .....	90
Multiplier, Capacitance (III.72) .....	98			..... (III.63) .....	93		
Multiplier-Divider (II.30) .....	54			Square Root of Sum of the Squares (III.65) ..	94		
..... (II.31) .....	54			Square-Wave Generator, Simple (III.18) .....	72		
				Stability, Dynamic Achievement of (I.42) .....	42		

CHARACTERISTICS Typical at +25°C unless otherwise indicated		P25A	Q25AH	P35A	P35C	P45A	P45C	P45AL
1. Application features (See price list for selection guide)	Differential high input impedance low offset current	Differential wideband low offset current	Differential high input impedance low offset current	Differential high input impedance low offset voltage	Differential input current compensated high input impedance low offset voltage	Ultra wideband large output current	Ultra wideband large output current input current compensated	Large output current
2. Voltage gain (dc open loop) At +25°C, rated load, minimum 10 kΩ load, minimum 100 kΩ load, minimum At -25°C, rated load, minimum At +85°C, rated load, minimum	40,000 80,000 150,000 30,000 60,000	10,000 20,000 80,000 7,500 7,500	100,000 200,000 1,000,000 40,000 150,000	100,000 200,000 1,000,000 40,000 150,000	50,000 200,000 200,000 20,000 100,000	50,000 200,000 200,000 20,000 100,000	50,000 200,000 200,000 20,000 100,000	50,000 200,000 200,000 20,000 100,000
3. Response (open loop, inverting, 25°C) Small signal: Unity gain-bandwidth minimum Gain at 1.0 MHz Large signal: Full output minimum Rate limit,	1.5 MHz 2 10 KHz 0.6 V/μ-sec	30 MHz 40 0.1 MHz 6.3 V/μ-sec	4 MHz 6 8 KHz 0.5 V/μ-sec	4 MHz 6 8 KHz 0.5 V/μ-sec	100 MHz 140 300 KHz 200 V/μ-sec	100 MHz 140 300 KHz 200 V/μ-sec	1.5 MHz 2 10 KHz 0.6 V/μ-sec	
4. Input voltage range Voltage range, both inputs Voltage range, between inputs, absolute maximum CMRR (dc, 25°C), minimum	±10 V 10 V 1000:1	±10 V 10 V 5,000:1	±10 V 5 V 20,000:1	±10 V 5 V 20,000:1	±10 V 5 V 1000:1	±5 V 5 V 300:1	±10 V 5 V 1000:1	
5. Input impedance Between inputs Negative input to common Positive input to common	10 <sup>12</sup> Ω    6 pF 10 <sup>12</sup> Ω    6 pF 10 <sup>12</sup> Ω    6 pF	10 <sup>12</sup> Ω    3 pF 10 <sup>12</sup> Ω    6 pF 10 <sup>12</sup> Ω    6 pF	5 MΩ    5 pF 2.10 <sup>9</sup> Ω    27 pF 2.10 <sup>9</sup> Ω    27 pF	5 MΩ    5 pF 2.10 <sup>9</sup> Ω    27 pF 2.10 <sup>9</sup> Ω    27 pF	220 kΩ    6 pF 33 MΩ    0.01μF 33 MΩ    6 pF	220 kΩ    6 pF 15 MΩ    0.01μF 15 MΩ    6 pF	220 kΩ    6pF 33 MΩ    1000pF 33 MΩ    6pF	
6. Input voltage offset Adjustment Vs Temp. (+10°C to +60°C), maximum Vs Temp. (-25°C to +85°C), maximum Vs Time (per day), Vs Time (½ hour),	Built-in 3 mV 6 mV 50 μV 10 μV	External 3 mV 6 mV 50 μV 10 μV	Built-in 1 mV 3 mV 25 μV 10 μV	Built-in 1 mV 3 mV 25 μV 10 μV	Built-in 2.5 mV 6 mV 100 μV 15 μV	Built-in 2.5 mV 6 mV 100 μV 15 μV	Built-in 2.5 mV 6 mV 100 μV 15 μV	
7. Input current offset 25°C, Vs Temp. (+10°C to +60°C), maximum Vs Temp. (-25°C to +85°C), maximum Vs Time (per day), Vs Time (½ hour),	0 (-) 150 pA * 1 nA 10 nA 3 pA 1 pA	0 (-) 150 pA 1 nA 10 nA 3 pA 1 pA	0 (+) 20 nA * 20 nA 45 nA 1 nA 0.1 nA	±4 nA * 4 nA 10 nA 1 nA 0.1 nA	±100 nA* 300 nA 1.2 nA 30 nA 3 nA	±50 nA * 50 nA 150 nA 30 nA 3 nA	±100 nA* 300 nA 1.2 nA 30 nA 3 nA	
8. Input noise (a) Flicker (0.016 to 1.6 Hz) voltage p-p current p-p (b) Broadband (160 to 16 KHz) Voltage rms Current rms	5 μV 2 pA 2 μV 3 pA	5 μV 2 pA 2 μV 3 pA	10 μV 0.05 nA 10 μV 6 pA	10 μV 0.05 nA 10 μV 6 pA	5 μV 0.5 nA 1 μV 600 pA	5 μV 0.5 nA 1 μV 600 pA	5 μV 0.5 nA 1 μV 60 pA	
9. Output (-25°C to +85°C) Voltage Current Load (rated)	±11 V ±22 mA 5 kΩ	±11 V ±22 mA 5 kΩ	±11 V ±22 mA 5 kΩ	±11 V ±22 mA 5 kΩ	±10 V ±20 mA 500 Ω	±10 V ±20 mA 500 Ω	±10 V ±20 mA 500 Ω	
10. Power requirements (+25°C), ± Voltage Current at +15 V (Quiescent) Current at +15 V (Full load) Current at -15 V (Quiescent) Current at -15 V (Full load)	±15 V 4.6 mA 4.6 mA 4.6 mA 6.8 mA	±15 V 6.6 mA 6.6 mA 6.6 mA 8.8 mA	±15 V 6 mA 6 mA 6 mA 8.2 mA	±15 V 6 mA 6 mA 6 mA 8.2 mA	±15 V 4 mA 23 mA 4 mA 23 mA	±15 V 4 mA 23 mA 4 mA 23 mA	±15 V 4 mA 23 mA 4 mA 23 mA	
11. Temperature range (in degrees Centigrade) Operating: Best overall Performance & Reliability Rated Maximum with derated specifications Storage: Maximum	-25 to +60 -25 to +85 -55 to +100 -62 to +125	-25 to +60 -25 to +85 -55 to +100 -62 to +125	0 to +60 -25 to +85 -55 to +100 -62 to +125	0 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +55 -25 to +85 -55 to +100 -62 to +125	
12. Alternate forms These units belong in the same family as the prototype because they have nearly equivalent circuit configurations. They may differ significantly from the listed types in electrical or physical characteristics, or applications considerations. Philbrick Researches welcomes your inquiry regarding these and other modified forms of standard units.	P25C and PP25C ■ have input currents approximately 1/10 of those given for P25A at any given temperature. P25A ■	P25AH is a plug-in version having similar performance. P154	P35A1 and PP35A1 ■ are units selected for less than 1 mV input voltage offset (-25°C to +85°C). PP35A ■	P35C1 and PP35C1 ■ are units selected for less than 1 mV input voltage offset (-25°C to +85°C). PP35C ■	P45 ■	PP45C ■	PP45L ■	
13. Price (quantity 1-4) Price of "Alternate Forms" may be slightly different. Prices may change without notice.	\$135	\$180	\$118	\$138	\$118	\$133	\$95	
14. Utility grade Where indicated, a utility grade equivalent, denoted by the letter U following the model designation, is available at reduced price. Utility grade amplifiers have identical performance with their premium grade equivalents in the temperature range 0-60°C. Storage temperatures below -55°C and above +85°C and certified test data are not available.	P25AU PP25AU ■ \$98		P35AU PP35AU ■ \$78		P45AU PP45U ■ \$89		P45LU PP45LU ■ \$65	
15. Outline Dimensions	P	Q	P	P	P	P	P	

**Suggested booster types** (used with operational amplifiers for voltage or current boost, connected inside the loop)  
**P56A** delivers ±10 V at ±100 mA with external "Boost" resistors connected; ±20 mA without.  
**PP56A** delivers same power output as Model P56A.  
**P5** delivers ±10 V at ±20 mA; physical companion of P2A.  
**6154-50/50** delivers ±50 V at ±50 mA with external "Boost" resistors connected; ±10 mA without; has dc gain of 7; requires ±60 V supplies.  
**05P8-100/10** delivers ±100 V at ±10 mA with external "Boost" resistors connected; ±1.5 mA without; has dc gain of 20; requires ±120 VDC supplies.

**Physical Form** Price (quantity 1-4)  
**P** \$39  
**PP** \$40  
**P2A** \$48  
**SP** \$85  
**PP56A**  
**P5**  
**6154-50/50**  
**05P8-100/10**



# SOLID STATE OPERATIONAL

P45CL	P55A	P65A	P65C	P65AH	P65Q	P75A	P85A	P85C	Q85AH
Large input current compensated	Differential low cost premium-grade construction	Differential versatile	Differential versatile input current compensated	Wideband versatile	Low quiescent power	High input impedance	Differential low voltage offset	Differential low voltage offset input current compensated	Differential wideband low voltage offset
50,000 200,000 200,000 20,000 100,000	20,000 40,000 40,000 5,000 35,000	20,000 40,000 80,000 10,000 40,000	20,000 40,000 80,000 10,000 40,000	20,000 40,000 80,000 10,000 40,000	20,000 100,000 10,000 40,000	20,000 40,000 80,000 10,000 40,000	50,000 100,000 200,000 20,000 60,000	50,000 100,000 200,000 20,000 60,000	20,000 40,000 80,000 15,000 15,000
1.5 MHz 2 10 kHz 0.6 V/ $\mu$ -sec	1.5 MHz 3 20 kHz 1.5 V/ $\mu$ -sec	1.5 MHz 3 20 kHz 1.5 V/ $\mu$ -sec	1.5 MHz 3 20 kHz 1.5 V/ $\mu$ -sec	20 MHz 25 75 kHz 5 V/ $\mu$ -sec	1.3 MHz 1.5 7.5 kHz 0.5 V/ $\mu$ -sec	1.5 MHz 3 20 kHz 1.5 V/ $\mu$ -sec	2 MHz 3 10 kHz 0.6 V/ $\mu$ -sec	2 MHz 3 10 kHz 0.6 V/ $\mu$ -sec	30 MHz 50 0.1 MHz 6.3 V/ $\mu$ -sec
$\pm 5$ V 5 V 300:1	$\pm 10$ V 5 V 1000:1	$\pm 10$ V 5 V 1000:1	$\pm 5$ V 5 V 300:1	$\pm 10$ V 5 V 1000:1	$\pm 10$ V 5 V 1000:1	$\pm 10$ V 5 V 1000:1	$\pm 11$ V 5 V 20,000:1	$\pm 11$ V 5 V 20,000:1	$\pm 11$ V 8 V 20,000:1
220 k $\Omega$    6 pF 15 M $\Omega$    1000 pF 15 M $\Omega$    6 pF	110 k $\Omega$    7 pF 15 M $\Omega$    400 pF 15 M $\Omega$    8 pF	220 k $\Omega$    6 pF 33 M $\Omega$    400 pF 33 M $\Omega$    6 pF	220 k $\Omega$    6 pF 15 M $\Omega$    400 pF 15 M $\Omega$    6 pF	220 k $\Omega$    6 pF 33 M $\Omega$    400 pF 33 M $\Omega$    6 pF	220 k $\Omega$    6 pF 33 M $\Omega$    400 pF 33 M $\Omega$    6 pF	10 M $\Omega$    6 pF 500 M $\Omega$    400 pF 500 M $\Omega$    6 pF	330 k $\Omega$    6 pF 88 M $\Omega$    6 pF 88 M $\Omega$    6 pF	330 k $\Omega$    6 pF 500 M $\Omega$    6 pF 500 M $\Omega$    6 pF	2 M $\Omega$    3 pF 500 M $\Omega$    5 pF 500 M $\Omega$    5 pF
Built-in 2.5 mV 6 mV 100 $\mu$ V 15 $\mu$ V	External 5 mV 20 mV 100 $\mu$ V 25 $\mu$ V	Built-in 1.5 mV 6 mV 50 $\mu$ V 10 $\mu$ V	Built-in 1.5 mV 6 mV 50 $\mu$ V 10 $\mu$ V	Built-in 1.5 mV 6 mV 50 $\mu$ V 10 $\mu$ V	Built-in 1.5 mV 6 mV 50 $\mu$ V 10 $\mu$ V	Built-in 3 mV 12 mV 100 $\mu$ V 25 $\mu$ V	Built-in 1 mV 3 mV 50 $\mu$ V 10 $\mu$ V	Built-in 1 mV 3 mV 50 $\mu$ V 10 $\mu$ V	External 1 mV 3 mV 50 $\mu$ V 10 $\mu$ V
$\pm 50$ nA* 50 nA 150 nA 30 nA 3 nA	$\pm 200$ nA* 1 $\mu$ A 3 $\mu$ A 100 nA 20 nA	$\pm 100$ nA* 400 nA 12 $\mu$ A 10 nA 1 nA	$\pm 50$ nA* 30 nA 150 nA 10 nA 1 nA	$\pm 100$ nA* 400 nA 12 $\mu$ A 10 nA 1 nA	$\pm 100$ nA* 200 nA 800 nA 5 nA 0.5 nA	(0+) 20 nA* 20 nA 60 nA 1 nA 0.1 nA	$\pm 50$ nA* 200 nA 440 nA 5 nA 0.5 nA	$\pm 50$ nA* 200 nA 150 nA 5 nA 0.5 nA	200 nA 200 nA 440 nA 3 nA 0.5 nA
5 $\mu$ V 0.5 nA 1 $\mu$ V 60 pA	15 $\mu$ V 1 nA 2 $\mu$ V 100 pA	10 $\mu$ V 0.5 nA 1 $\mu$ V 60 pA	10 $\mu$ V 0.5 nA 1 $\mu$ V 60 pA	10 $\mu$ V 0.5 nA 1 $\mu$ V 60 pA	10 $\mu$ V 0.5 nA 1 $\mu$ V 60 pA	20 $\mu$ V 0.05 nA 10 $\mu$ V 6 pA	5 $\mu$ V 0.25 nA 1 $\mu$ V 30 pA	5 $\mu$ V 0.25 nA 1 $\mu$ V 30 pA	5 $\mu$ V 0.25 nA 1 $\mu$ V 30 pA
$\pm 10$ V $\pm 20$ mA 300 $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$	$\pm 11$ V $\pm 0.5$ mA 20 k $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$	$\pm 11$ V $\pm 22$ mA 5 k $\Omega$
$\pm 15$ V 4 mA 23 mA 23 mA 23 mA	$\pm 15$ V 5.5 mA 7.7 mA 5.5 mA 5.5 mA	$\pm 15$ V 5.5 mA 7.7 mA 5.5 mA 5.5 mA	$\pm 15$ V 5.5 mA 7.7 mA 5.5 mA 5.5 mA	$\pm 15$ V 5.5 mA 7.7 mA 5.5 mA 5.5 mA	$\pm 15$ V 0.9 mA 1.45 mA 0.9 mA 0.9 mA	$\pm 15$ V 5.5 mA 7.7 mA 5.5 mA 5.5 mA	$\pm 15$ V 4 mA 4 mA 4 mA 6.2 mA	$\pm 15$ V 4 mA 4 mA 4 mA 6.2 mA	$\pm 15$ V 6 mA 6 mA 6 mA 8.2 mA
+10 to +55 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125	+10 to +60 -25 to +85 -55 to +100 -62 to +125
<b>P45CL</b> ■	<b>P55AH</b> and <b>P55ASAH</b> ■ are stable wide-band versions \$53	<b>P65SAH</b> ■ uses millilary transistor types.	<b>P65QAH</b> and <b>P65QCH</b> ■ are wideband versions \$79	<b>P65AH</b> ■	<b>P65QC</b> and <b>P65QSC</b> ■ have temperature sensitive input current compensation; lower common mode voltage range and C.M.R.R.	<b>PP75AH</b> ■	<b>P85AH</b> and <b>P85ASAH</b> ■ are units selected for less than 1 mV input voltage offset (-25°C to +85°C).	<b>PP85AH</b> ■	<b>P85AH</b> is a discrete component plug-in version having similar performance. \$38
<b>P55AH</b> ■ <b>P55ASAH</b> ■ <b>P55AH</b> ■ <b>P55ASAH</b> ■ <b>P55AH</b> ■	<b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■	<b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■	<b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■	<b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■	<b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■ <b>P65ASAH</b> ■ <b>P65AH</b> ■	<b>P75AH</b> ■ <b>PP75AH</b> ■ <b>P75AH</b> ■ <b>PP75AH</b> ■ <b>P75AH</b> ■	<b>P85AH</b> ■ <b>P85ASAH</b> ■ <b>P85AH</b> ■ <b>P85ASAH</b> ■ <b>P85AH</b> ■	<b>P85AH</b> ■ <b>P85ASAH</b> ■ <b>P85AH</b> ■ <b>P85ASAH</b> ■ <b>P85AH</b> ■	<b>P85AH</b> ■ <b>P85ASAH</b> ■ <b>P85AH</b> ■ <b>P85ASAH</b> ■ <b>P85AH</b> ■
\$21.50 \$20 \$20 \$23.50 \$24	\$33 \$30	\$37 \$34	\$37 \$34	\$68	\$49	\$68	\$49	\$49	\$161
\$110	\$49	\$65	\$80	\$69	\$69	\$38	\$75	\$95	\$161

LEGEND  
M—mega—10<sup>6</sup>  
K—kilo—10<sup>3</sup>  
m—milli—10<sup>-3</sup>  
 $\mu$ —micro—10<sup>-6</sup>  
n—nano—10<sup>-9</sup>  
p—pico—10<sup>-12</sup>  
f—femto—10<sup>-15</sup>

# AMPLIFIERS

CHARACTERISTICS Typical at +25°C unless otherwise indicated					
1. Application features (See price list for selection guide)	SP456†	SP656†	SP65AH†	SP65A†	SP2A
2. Voltage gain (dc open loop) At +25°C, rated load, minimum 10 k $\Omega$ load, minimum 100 k $\Omega$ load, minimum At -25°C, rated load, minimum At +85°C, rated load, minimum	4 x 10 <sup>5</sup> 10 <sup>5</sup> 4 x 10 <sup>5</sup> 5 x 10 <sup>5</sup> 2 x 10 <sup>5</sup>	5 x 10 <sup>7</sup> 10 <sup>6</sup> 2 x 10 <sup>7</sup> 2.3 x 10 <sup>7</sup> 10 <sup>6</sup>	10 <sup>7</sup> 2 x 10 <sup>7</sup> 4 x 10 <sup>7</sup> 5 x 10 <sup>6</sup> 4 x 10 <sup>7</sup>	10 <sup>7</sup> 2 x 10 <sup>7</sup> 4 x 10 <sup>7</sup> 5 x 10 <sup>6</sup> 4 x 10 <sup>7</sup>	20,000 40,000 150,000 10,000 (0°C) 10,000 (65°C)
3. Response (open loop, inverting, 25°C) Small signal: Unity gain-bandwidth minimum Gain at 1.0 MHz Large signal: Full output Rate limit.	100 MHz 140 14 300 kHz 200 V/ $\mu$ -sec	1.5 MHz 3 20 kHz 75 kHz 5 V/ $\mu$ -sec	20 MHz 25 25 75 kHz 5 V/ $\mu$ -sec	1.5 MHz 3 20 kHz 1.5 V/ $\mu$ -sec	75 kHz — 1.1 kHz .066 V/ $\mu$ -sec
4. Input voltage range Voltage range, both inputs Voltage range, between inputs, absolute maximum CMRR (dc, 25°C), minimum	$\pm$ 0.1 V 0.5 V —	$\pm$ 0.1 V 0.5 V —	$\pm$ 0.1 V 0.5 V —	$\pm$ 0.1 V 0.5 V —	$\pm$ 200 V 15 V Infinite
5. Input impedance Between inputs Negative input to common Positive input to common	—	—	—	—	10 <sup>10</sup> $\Omega$    500pF 10 <sup>12</sup> $\Omega$    5pF 10 <sup>12</sup> $\Omega$    5pF
6. Input voltage offset Adjustment Vs Temp. (+10°C to +60°C), maximum Vs Temp. (-25°C to +85°C), maximum Vs Time (per day), Vs Time (½ hour),	20 $\mu$ V (5 $\mu$ V typ.), 50 $\mu$ V (20 $\mu$ V typ.) 1 $\mu$ V 1 $\mu$ V	20 $\mu$ V (5 $\mu$ V typ.), 50 $\mu$ V (20 $\mu$ V typ.) 1 $\mu$ V 1 $\mu$ V	20 $\mu$ V (5 $\mu$ V typ.), 50 $\mu$ V (20 $\mu$ V typ.) 1 $\mu$ V 1 $\mu$ V	20 $\mu$ V (5 $\mu$ V typ.), 50 $\mu$ V (20 $\mu$ V typ.) 1 $\mu$ V 1 $\mu$ V	Built-in 6 mV (0-65°C) 100 $\mu$ V 10 $\mu$ V
7. Input current offset 25°C Vs Temp. (+10°C to +60°C), maximum Vs Temp. (-25°C to +85°C), maximum Vs Time (per day), Vs Time (½ hour),	10 pA 30 pA 100 pA 10 pA 2 pA	10 pA 30 pA 100 pA 10 pA 2 pA	10 pA 30 pA 100 pA 10 pA 2 pA	10 pA 30 pA 100 pA 10 pA 2 pA	$\pm$ 10 pA 100 pA (0-65°C) 0.1 pA 0.01 pA
8. Input noise (a) Flicker (0.016 to 16 Hz) voltage p-p (b) Broadband (160 to 16 kHz) Voltage rms Current rms	6 $\mu$ V 0.1 nA 1 $\mu$ V 600 pA	6 $\mu$ V 0.1 nA 1 $\mu$ V 60 pA	6 $\mu$ V 0.1 nA 1 $\mu$ V 60 pA	6 $\mu$ V 0.1 nA 1 $\mu$ V 60 pA	1 $\mu$ V 1 nA 10 $\mu$ V 500 pA
9. Output (-25°C to +85°C) Voltage Current Load (rated)	$\pm$ 10 V $\pm$ 20 mA 500 $\Omega$	$\pm$ 10 V $\pm$ 20 mA 500 $\Omega$	$\pm$ 11 V $\pm$ 22 mA 5 k $\Omega$	$\pm$ 11 V $\pm$ 22 mA 5 k $\Omega$	$\pm$ 11 V $\pm$ 22 mA 5 k $\Omega$
10. Power requirements (+25°C) $\pm$ Voltage Current at +15 V (Quiescent) Current at +15 V (Full load) Current at -15 V (Quiescent) Current at -15 V (Full load)	$\pm$ 15 V 5 mA 24.5 mA 4.5 mA 24 mA	$\pm$ 15 V 8.75 mA 28 mA 8.75 mA 28.5 mA	$\pm$ 15 V 8 mA 10 mA 7 mA 7 mA	$\pm$ 15 V 8 mA 10 mA 7 mA 7 mA	$\pm$ 15 V 8 mA 10 mA 7 mA 8.2 mA
11. Temperature range (in degrades Centigrade) Operating: Best overall Performance & Reliability Rated Maximum Storage: Maximum	+10 to +60 -25 to +85 -45 to +85 -55 to +85	+10 to +60 -25 to +85 -45 to +85 -55 to +85	+10 to +60 -25 to +85 -45 to +85 -55 to +85	+10 to +60 -25 to +85 -45 to +85 -55 to +85	+10 to +40 0 to +65 -25 to +85 -45 to +85 -55 to +85
12. Alternate forms These units belong in the same family as the prototype because they have nearly equivalent circuit configurations. They may differ significantly from the listed types in electrical or physical characteristics, or applications considerations. Philbrick Researches welcomes your inquiry regarding these and other modified forms of standard units.					P2A is a wire-in version of SP2A. It has no provision for a driven guard. SP2B has 20 mA output current capability. SP2C has $\pm$ 100V @ 10 mA output capability. SP2S
13. Price (quantity 1-4) Price of "Alternate Forms" may be slightly different. Prices may change without notice.	\$227	\$195	\$189	\$180	\$227
14. Utility grade Where indicated, a utility grade equivalent, denoted by the letter U following the model designation, is available at reduced price. Utility grade amplifiers have identical performance with their premium grade equivalents in the temperature range 0-60°C. Storage temperatures below -55°C and above +85°C and certified test data are not available.					
15. Outline Dimensions					

\* P-models have built-in current trim resistors. These may be installed externally on P-models. See individual P- data sheets.

† Specifications shown are for units with mechanical chopper; 6.3 VAC, 50-80 cps at 80 mA is required. Units with photochopper are available for operation below +65°C. In addition to 6.3 VAC, 50-80 cps, 1 mA, the photochopper also requires 115 VAC, 5 mA, at the same frequency and phase.

‡ At +85°C power requirements will be 10% higher than those stated at +25°C. For maximum power requirements at any temperature add 10%.

◆ A compact wire-in cast epoxy version having similar performance. Voltage offset adjustment external.

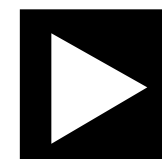
◆ A plug-in cast epoxy version having similar performance. Voltage offset adjustment external.

◆ With Trim 1 terminal grounded. Can be trimmed to zero by voltage bias ( $\pm$ 5 V Max.) applied to "Trim 1" terminal.





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